

# Intel Sky Lake Platform

## SLK-S CPU / SLK PCH-H

PAGE	TITLE
01	INDEX
02	BLOCK DIAGRAM
03	CLOCKS DIAGRAM
04	POWER DISTRIBUTION (FARALLON)
05	POWER MAP:SKYLAKE FOR DDR4
06	STRAP & GPIO
07	POWER DISTRIBUTION(SFF)
08	INTERRUPT & PME DIAGRAM
09	CPU XDP
10	CPU- CLK/ CTRL/ MISC/DEBUG
11	CPU- DDR3 CH A & B(SFF)
12	CPU-DDR4 CHA&B(Precision)
13	CPU- PCIE/ DMI/ DDI
14	CPU- VCC/VDDDQ
15	CPU- VSS
16	BLANK
17	DDR4 CHA0 DIMM3
18	DDR4 CHA1 DIMM1
19	DDR4 CHB0 DIMM4
20	DDR4 CHB1 DIMM2
21	PCH - DMI/ PCIE/ USB2/3##
22	PCH - SMBUS/HDA/GPIO/JTAG
23	PCH - SATA/SPI/GPIO
24	PCH - GPIO/MISC
25	PCH - CLOCK
26	PCH - POWER & GND
27	PCH-PLL FILTER&DECOUPLING
28	PCH-8:MISC CONN/BEEP/ID
29	SIO-1
30	SIO-2
31	LAN: Intel Jacksonville
32	LAN: RTK RTL8111HSD(SFF3)
33	LAN Power & LAN/USB Conn
34	Audio ALC3234
35	Audio Conn
36	Slot1: PCIE 1x (SFF3)
37	Slot2: PCIE 16x
38	Slot3: PCIE 4x(SFF7)
39	HDMI-1
40	Display PortC
41	Display PortD
42	SATA Conn
43	Rear USB3x4 (SFF7)
44	Rear USB3x2 (SFF3)
45	TPM
46	FAN & LABEL
47	PS2 Conn Option (SFF3)
48	PS2 Conn (SFF7)
49	THERMAL SENSOR (SFF3)
50	COM1&THERMAL SENSOR(SFF7)
51	SPI
52	PCH XDP##
53	Pilot Run/LPC Debug/APS
54	EMI
55	Front USB2(SFF7)
56	Front USB3
57	M2 card (SFF7 and Farallon)
58	SD4.0 CON/ DP TO VGA CONN
59	Power Sequence
60	Power Conn
61	Power-1: Linear Power-1
62	Power-2: Linear Power-2
63	Power-3: Linear Power-3
64	Power-4: +VCORE/+VCCGT


65	Power-5:+VCORE Driver
66	Power-6:+VCCGT Driver
67	Power-7:+VCCSA
68	Power-8:+VCCIO
69	Power-9+1P0V_PCH_AUX
70	Power-10:+3P3V_SB/+5V_AUX
71	Power-11:-12V
72	Power-12:DDR3 +1P35V_VDDQ
73	Power-13:DDR4 +1P2V_VDDQ
74	Power-14:DDR4 +VTT_DDR
75	Power-15:DDR4 +VPP
76	DDR3 Conn: CHA_0 (DIMM3)##
77	DDR3 Conn: CHA_1 (DIMM1)##
78	DDR3 Conn: CHB_0 (DIMM4)##
79	DDR3 Conn: CHB_1 (DIMM2)##
80	TBT & FAN (Farallon Only)
81	Front USB2 (SFF3)
82	DP PORTC(SFF3)
83	M2 card(SFF3)
84	POWER MAP:SKYLAKE FOR DDR3

www.aitech1.ru

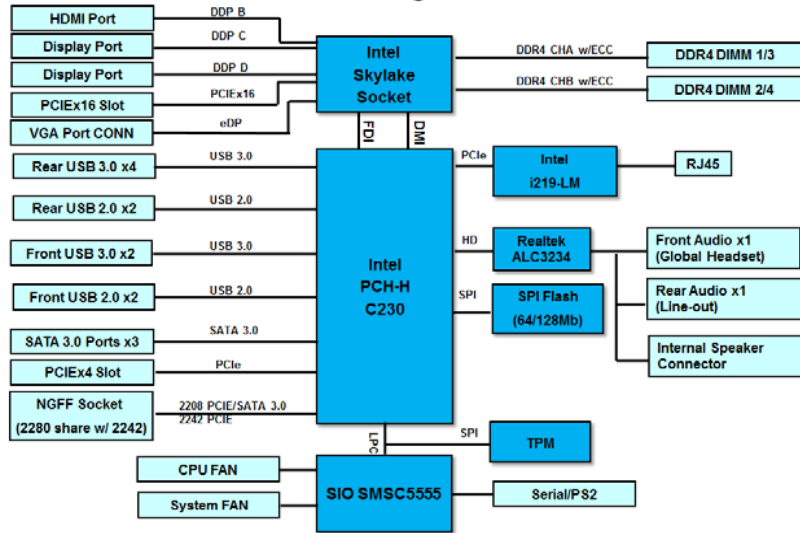
DO NOT DISTRIBUTE

Marking	Description
I	Installed
NI	Not Installed
MP	Production Part ONLY
PROTO	Not For Production Part
CCL	Critical Components List

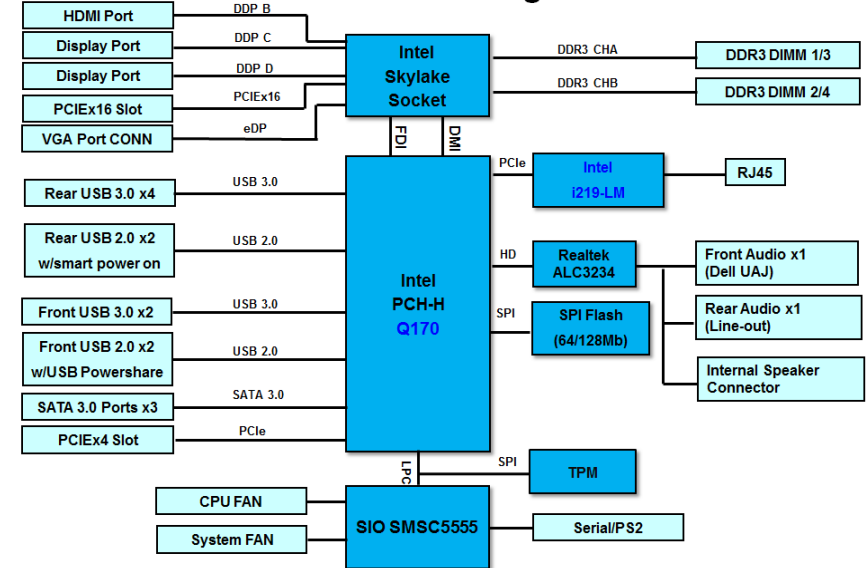
PCA P/N, Scorpion/Spitfire/Toledo	
SCH P/N, Scorpion/Spitfire/Toledo	
PCB P/N, Scorpion/Spitfire/Toledo	

	
INC.	
Title	
INDEX	
DWG NO	Rev
D7	X02
Date: Monday, July 27, 2015	Sheet 1 of 87

### Farallon SFF MB Block Diagram

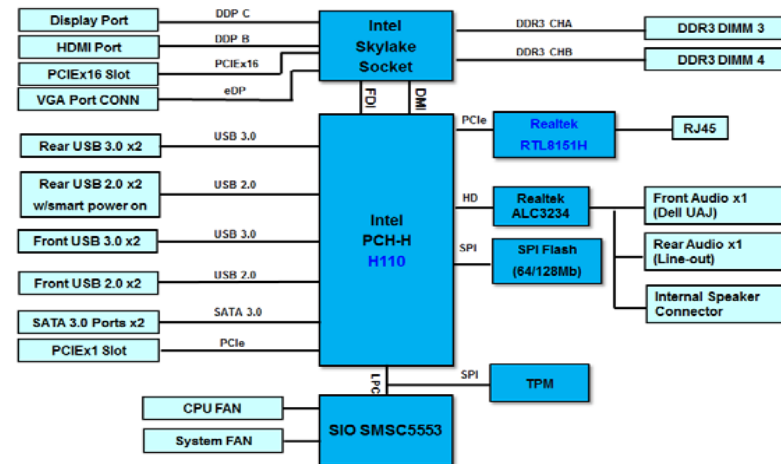


### Swordfish SFF 9 MB Block Diagram

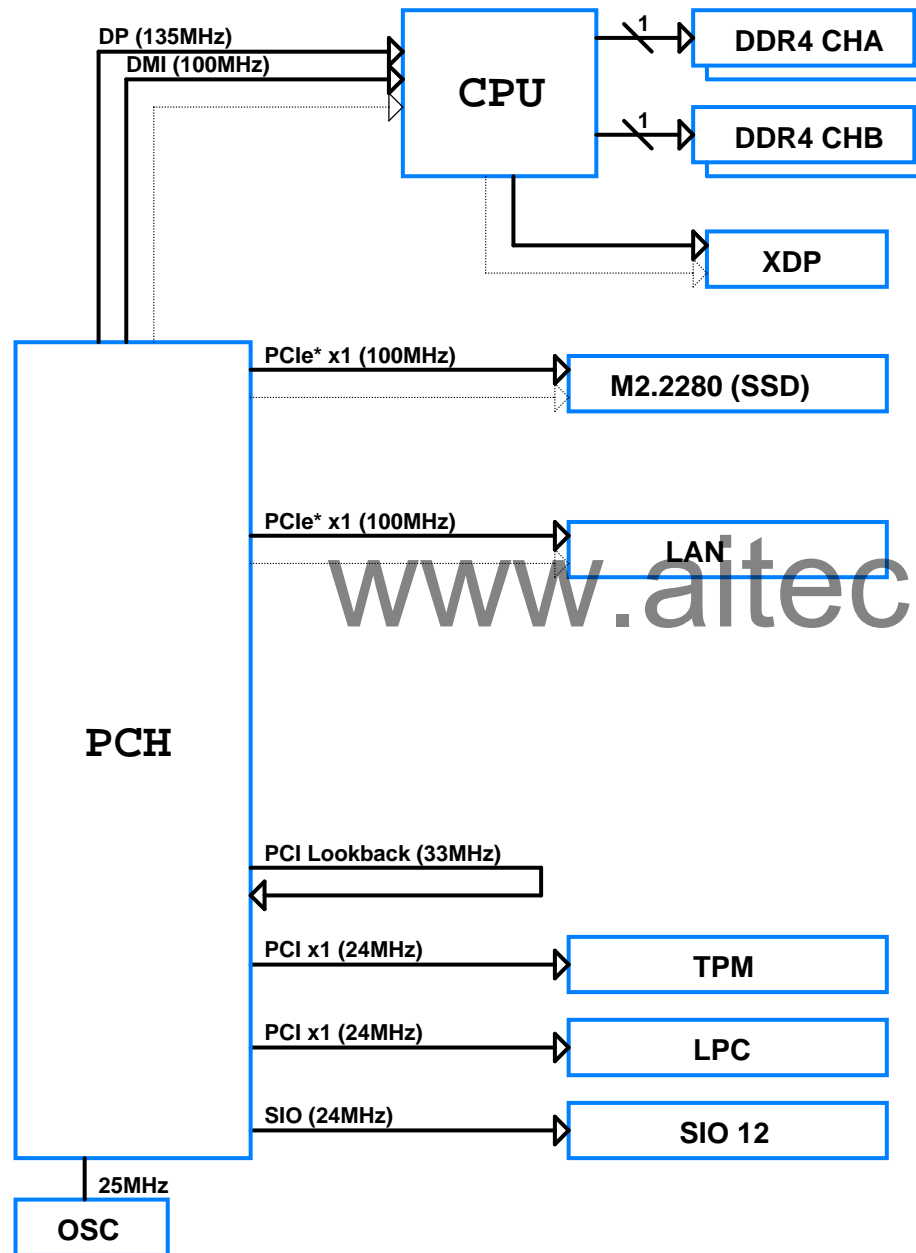


www.aitech1.ru

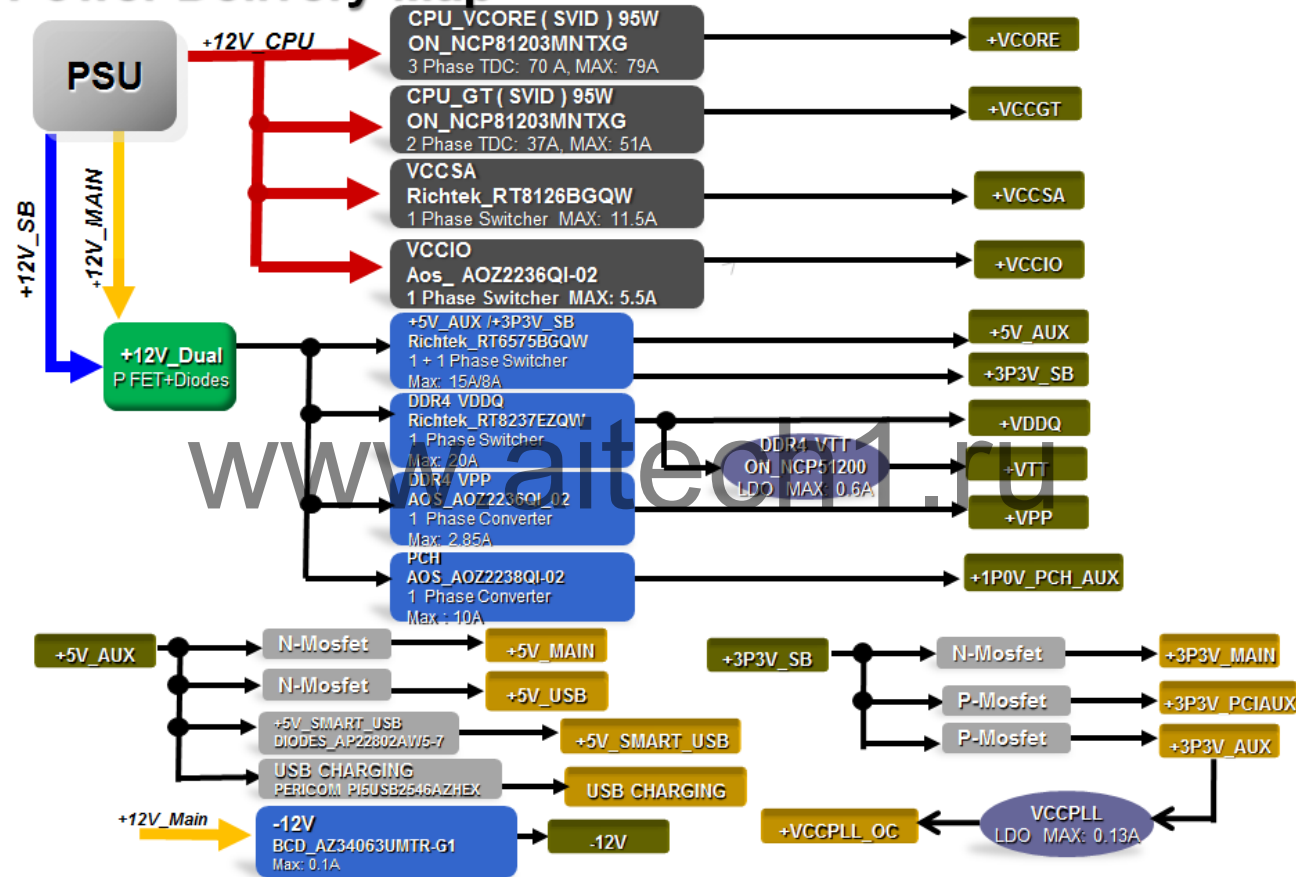
### Swordfish SFF 3 MB Block Diagram



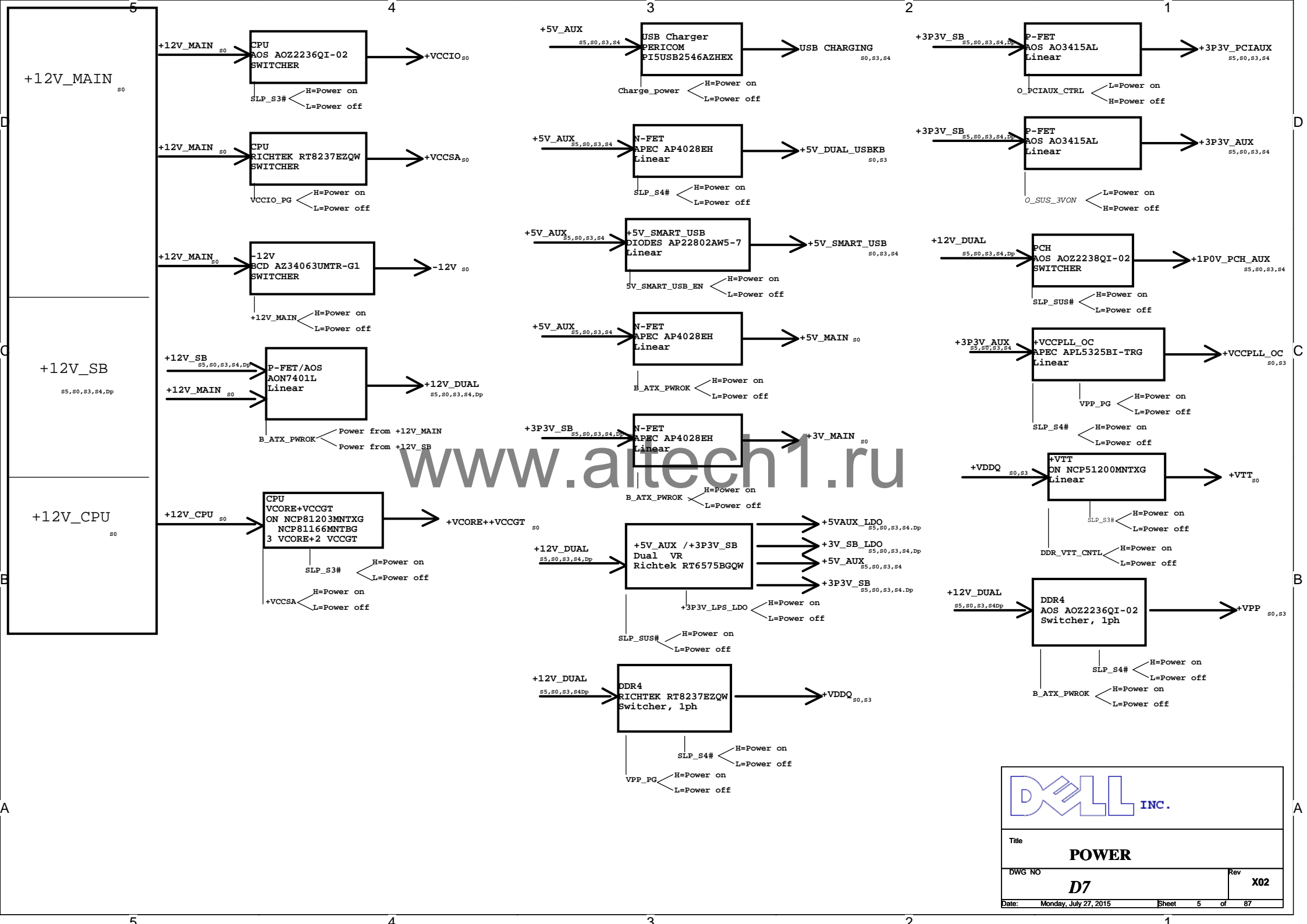
# Clock Diagram



# Power Delivery Map







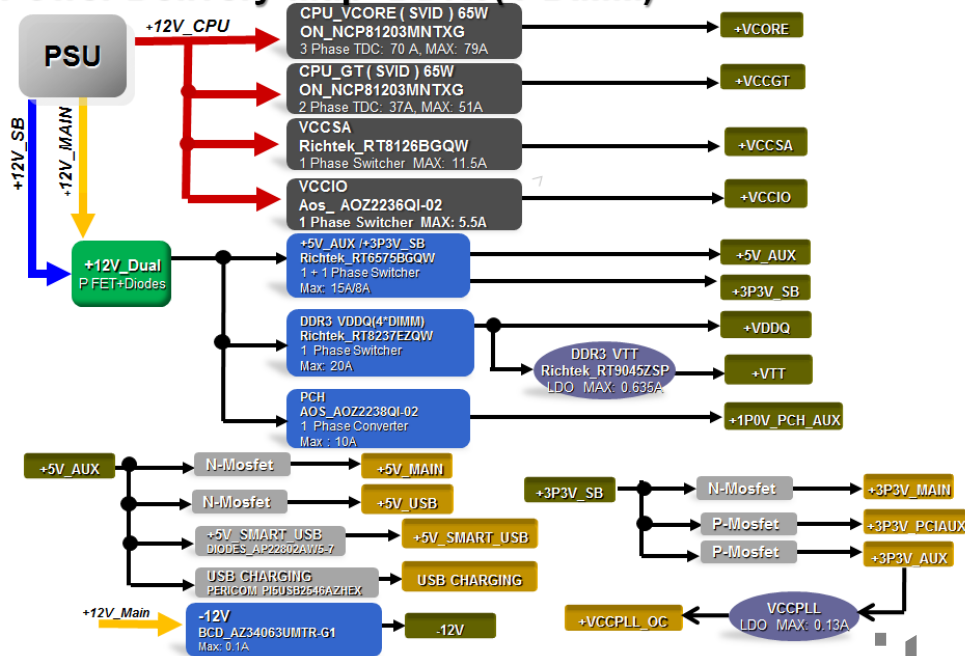
44	PCIECLKRQ05#	--	20k Pu <sup>5</sup>	I/O 3.3	Sus	N	1	2	Z	Q	D	Q	Q	PCIE_RISER_DET#	G	1	--
43	OC#4#	--	--	I/O 3.3	Sus	N	1	2	Z	Q	D	Q	Q	PASSWORD_EN	G	1	--
42	OC#3#	--	--	I/O 3.3	Sus	N	1	2	Z	Q	D	Q	Q	OC#3#	N	1	--
41	OC#2#	--	--	I/O 3.3	Sus	N	1	2	Z	Q	D	Q	Q	OC#2#	N	1	--
40	OC#1#	--	--	I/O 3.3	Sus	N	1	2	Z	Q	D	Q	Q	OC#1#	N	1	--
39	SDATAQ10T0	--	--	I/O 3.3	Core	G	1	2	Z	Q	D	Q	Q	BRD_ID1	G	1	--
38	SLOAD	--	--	I/O 3.3	Core	G	1	2	Z	Q	D	Q	Q	CHASSIS_ID0	G	1	--
37	SATAG3P	TLS Conf.	20k Pu <sup>1</sup>	I/O 3.3	Core	G	1	0	2	D	--	--	--	Rxd	G	1	--
36	SATAG3P	Rxd	20k Pu <sup>1</sup>	I/O 3.3	Core	G	1	0	2	D	--	--	--	Rxd	G	1	--
35	S_NMI#	--	--	I/O 3.3	Core	G	1	2	1	1	1	--	--	BRD_REV	G	1	--
34	--	--	--	I/O 3.3	Core	G	1	2	Z	Q	D	Q	Q	HOOD_LOCK_DET	G	1	--
33	M: HAD_DOCK_EN#	Rxd	--	I/O 3.3	Core	G	0	0	0	0	1	--	--	Rxd	G	1	--
32	--	--	--	I/O 3.3	Core	G	0	1	1	1	1	--	--	PWR_COMB_CFG0	G	0	1
31	M: AC_PRESENT	--	20k Pd <sup>3</sup>	I/O 3.3	DSW	G	1	2	Z	Q	D	Q	Q	Rxd	G	1	--
30	SUSWRN# / SLF_PWRDNACK	--	--	I/O 3.3	Sus	N	0	1	0	1	0	D	Q	SUSWRN#	N	0	x
29	SUP_WLN#	--	--	I/O 3.3	DSW	G	0	0	0	1	0	D	Q	SLF_WLN#	N	0	x
28	--	--	--	I/O 3.3	Sus	G	0	0	0	0	0	--	--	PWR_COMB_CFG0	G	0	0
27	--	--	20k Pd <sup>3</sup>	I/O 3.3	DSW	G	1	2	Z	Q	Z	Q	Z	DSW_WOL_WAKE	G	1	--
26	PCIECLKRQ4#	--	--	I/O 3.3	Sus	N	1	2	Z	Q	D	Q	Q	PWR_SER_DET#	G	1	--
25	PCIECLKRQ3#	--	--	I/O 3.3	Sus	N	1	2	Z	Q	D	Q	Q	BRD_ID2	G	1	--
24	--	--	--	I/O 3.3	Sus	G	0	0	0	0	0	D	Q	PWR_COMB_CFG0	G	0	0
23	LDRQ1#	--	20k Pu <sup>1</sup>	I/O 3.3	Core	N	1	2	Z	Q	D	Q	Q	LDRQ1#	N	1	--
22	SCLOCK	--	--	I/O 3.3	Core	G	1	2	Z	Q	D	--	--	INT_USR_DET#	G	1	--
21	SATAG3P	--	--	I/O 3.3	Core	G	1	2	Z	Q	D	--	--	FRNT_AUD_DET#	G	1	--
20	PCIECLKRQ2	S_NMI#	--	I/O 3.3	Core	G	1	2	Z	Q	--	--	--	PCIECLKRQ2#	N	1	--
19	SATAG1P	BBSD	20k Pu <sup>1</sup>	I/O 3.3	Core	G	1	1	2	Q	--	--	--	Rxd	G	1	--
18	PCIECLKRQ1#	--	--	I/O 3.3	Core	N	1	2	Z	Q	D	--	--	MMX_PWR_GD#	G	1	--
17	S: TACH0	--	20k Pu <sup>2</sup>	I/O 3.3	Core	G	1	2	Z	Q	D	--	--	HOOD_SW_DET#	G	1	--
16	SATAG3P	--	--	I/O 3.3	Core	G	1	2	Z	Q	D	--	--	Rxd	G	1	--
15	--	--	--	I/O 3.3	Sus	G	0	0	0	0	Q	D	Q	WRITE_EDD_ROM	G	0	0
14	OC#7#	--	--	I/O 3.3	Sus	N	1	2	Z	Q	D	Q	Q	OC#7#	N	1	--
13	M: HAD_DOCK_RST#	--	--	I/O 3.3	Sus	G	1	2	Z	Z	Z	Z	--	INT_USR_DET#	G	1	--
12	CAN_PPT_PWR_CTRL	--	--	I/O 3.3	Sus	N	0	1	0	1	0	--	--	CAN_DISABLE#	N	0	x
11	SMBA1#	--	--	I/O 3.3	Sus	N	0	1	0	1	0	--	--	CSB_RESET#	N	0	x
10	OC#6#	--	--	I/O 3.3	Sus	N	1	2	Z	Q	D	D	Q	OC#6#	N	1	--
9	OC#5#	--	--	I/O 3.3	Sus	N	1	2	Z	Q	D	D	Q	OC#5#	N	1	--
8	--	Rxd	20k Pu <sup>6</sup>	I/O 3.3	Sus	G	0	1	1	Q	D	D	Q	Rxd	G	1	--
7	S: TACH3	--	20k Pu <sup>2</sup>	I/O 3.3	Core	G	1	2	Z	Q	D	--	--	MMX_TH_ALERT#	G	1	--
6	S: TACH2	--	20k Pu <sup>2</sup>	I/O 3.3	Core	G	1	2	Z	D	--	--	--	SMI# from SIO#	G	1	--
5	PIRQ0#	--	--	I/O 0	S	Core	G	1	2	Z	D	--	--	GS_INT#	G	1	--
4	PIRQ0#	--	--	I/O 0	S	Core	G	1	2	Z	D	--	--	Rxd	G	1	--
3	PIRQ0#	--	--	I/O 0	S	Core	G	1	2	Z	D	--	--	MMX_RESET#	G	0	0
2	PIRQ0#	--	--	I/O 0	S	Core	G	1	2	Z	D	--	--	MMX_PWR_EN#	G	0	0
1	S: TACH1	--	20k Pu <sup>2</sup>	I/O 3.3	Core	G	1	2	Z	Q	D	--	--	MMX_TH_OVTR#	G	1	--
0	BIMBUS#	--	--	I/O 3.3	Core	G	1	2	Z	D	Q	--	--	FR_USR_DET#	G	1	--

Signal	Usage	When Sampled	Comment
			<p>This signal has a weak internal pull-up.</p> <p>0 = <b>Enable</b> "Top-Block Swap" mode - PCH will invert A16 for cycles going to the upper two 64 KiB blocks in the PWH or appropriate address lines (A16, A17, A18 A19 or A20) as selected in BIOS Boot-Block size soft strap for SPI.</p> <p>1 = <b>Disable</b> "Top-Block Swap" mode.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>The internal pull-up is disabled after PLTRST# deasserts.</li> <li>Software will not be able to clear the Top-Block Swap bit until the system is rebooted.</li> <li>This signal is in the Core well.</li> <li>The status of this strap is readable using the Top-Block Swap bit (Chipset Config Registers: RCBA + Offset 3414h-Bit 0).</li> </ol>
GPIOSS	Top-Block Swap Override	Rising edge of PWROK	
			<p>This signal has a weak internal pull-down.</p> <p>0 = Port B is not detected.</p> <p>1 = Port B is detected.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after PLTRST# deasserts.</li> </ol>
DOPB_CTRLDATA	Port B Detected	Rising edge of PWROK	
			<p>This signal has a weak internal pull-down.</p> <p>0 = Port C is not detected.</p> <p>1 = Port C is detected.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after PLTRST# deasserts.</li> </ol>
DOPC_CTRLDATA	Port C Detected	Rising edge of PWROK	
			<p>This signal has a weak internal pull-down.</p> <p>0 = Port D is not detected.</p> <p>1 = Port D is detected.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after PLTRST# deasserts.</li> </ol>
DOPD_CTRLDATA	Port D Detected	Rising edge of PWROK	

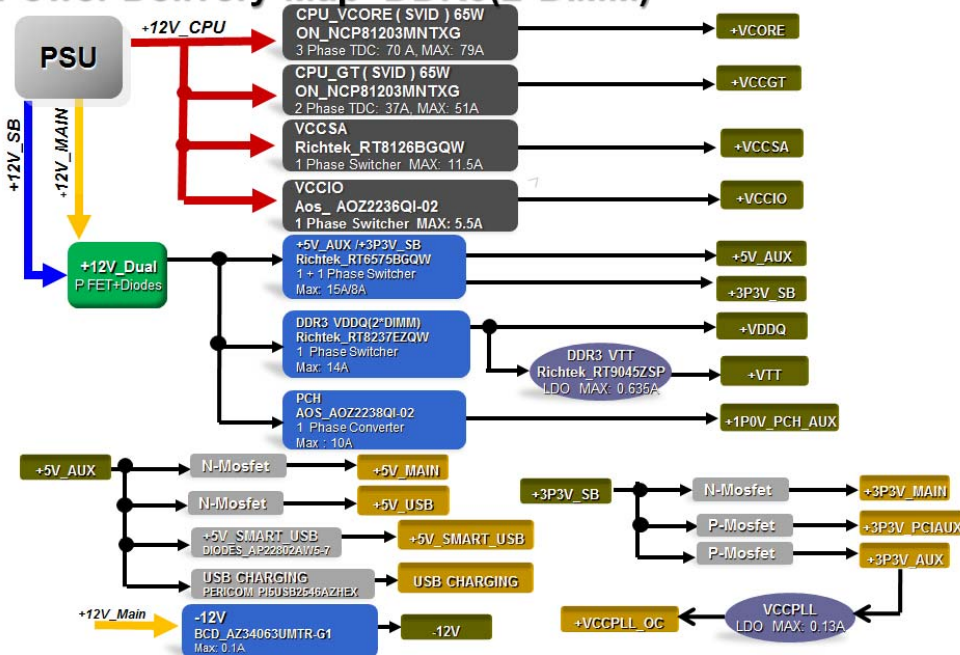
Signal	Usage	When Sampled	Comment
HDA_SDO	Flash Descriptor Security Override	Rising edge of PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Enable security measures defined in the Flash Descriptor</p> <p>1 = Disable Flash Descriptor Security (<i>override</i>). This strap should only be asserted high using external pull-up in manufacturing/debug environments <b>ONLY</b>.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>The weak internal pull-down is disabled after PLTRST# deasserts.</li> <li>Asserting the HDA_SDO high on the rising edge of PWROK will also halt Intel® Management Engine after chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.</li> <li>This signal is in the Suspend well.</li> </ol>
HDA_DOCK_EN# GPIO33	Reserved	Rising edge of PWROK	<p>This signal has a weak internal pull-down.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after PLTRST# deasserts.</li> <li>This signal should not be pulled high when strap is sampled.</li> </ol> <p>This signal does not have an internal resistor; an external resistor is <b>required</b>.</p> <p>0 = DCPUSU1, DCPUSU2 and DCPUSU3 are powered from an external power source (should be connected to an external VRM). External VRM powering option is for Mobile Only. Other systems should not pull the strap low.</p> <p>1 = Integrated VRMs enabled. DCPUSU1, DCPUSU2 and DCPUSU3 can be left floating.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>This signal is always sampled.</li> <li>This signal is in the RTC well.</li> </ol>
INTVRMEN	Integrated VRM Enable	Always	<p>This signal has a weak internal pull-up.</p> <p>0 = Disable PLL On-Die voltage regulator.</p> <p>1 = Enable PLL On-Die voltage regulator.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>The internal pull-up is disabled after RSMRST# deasserts.</li> <li>This signal is in the Suspend well.</li> </ol>
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	Rising edge of RSMRST#	<p>This signal has a weak internal pull-up.</p> <p>0 = Disable PLL On-Die voltage regulator.</p> <p>1 = Enable PLL On-Die voltage regulator.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>The internal pull-up is disabled after RSMRST# deasserts.</li> <li>This signal is in the Suspend well.</li> </ol>

Signal	Usage	When Sampled	Comment
D5WRMEN	DeepSleep Well On-Voltage Regulator Enable	Always	<p>This signal does not have an internal resistor; an external resistor is <b>required</b>.</p> <p><b>0 = Disable</b> Integrated DeepSleep Well (DSW) On-Die Voltage Regulator.</p> <p><b>1 = Enable</b> DSW 3.2V-to-1.05V Integrated DeepSleep Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards; the external mode is only used for testing environments.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>This signal is always sampled.</li> <li>This signal is in the RTC well.</li> </ol> <p>This signal has a weak internal pull-up but <b>requires an external pull down</b>.</p>
GPIO6	Reserved	Rising edge of RSMRST#	<p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>The internal pull-up is disabled after RSMRST# deasserts.</li> <li>This signal <b>must be pulled low</b> when strap is sampled.</li> <li>This signal is in the Suspend well.</li> </ol> <p>The signal has a weak internal pull-down.</p> <p><b>0 = Disable</b> "No Reboot" mode.</p> <p><b>1 = Enable</b> "No Reboot" mode (PCH will disable the TCO timer system reboot feature).</p>
SPKR	No Reboot	Rising edge of PWROK	<p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after PLTRST# deasserts.</li> <li>The status of this strap is readable using the <b>NO REBOOT</b> bit (Chipset Config Registers: RCBA + Offset: 3410h, Bit 5).</li> <li>See <b>Chapter 10, "GCS—General Control and Status Register"</b> for additional information.</li> <li>This signal is in the Core well.</li> </ol> <p>This signal has a weak internal pull-up.</p>
GPIO53	Reserved	Rising edge of PWROK	<p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>The internal pull-up is disabled after PLTRST# deasserts.</li> <li>This signal should not be pulled low when strap is sampled.</li> </ol>

## Power Delivery Map DDR3(4\*DIMM)



## Power Delivery Map DDR3(2\*DIMM)



www.aitech1.ru

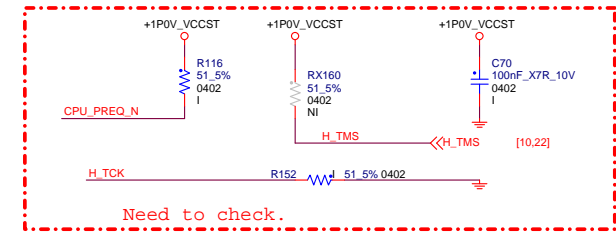
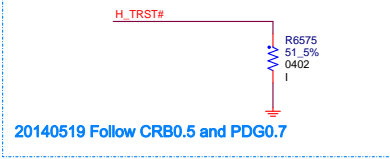


Title  
**Interrupt & PME**

DWG NO <b>D7</b>	Rev <b>X02</b>
---------------------	-------------------

Date: Monday, July 27, 2015	Sheet 8 of 87
-----------------------------	---------------

# 20140520 Need check Debug port PDG



## Intel MCP XDP Debug Connector

PREQ# and PRDY# MUST be routed in this order: Debug Port -> CPU -> PCH-H.  
place R148,R149 close to CPU  
20140520 Follow CRB0.5 and PDG0.7

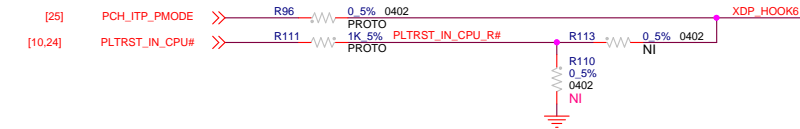
CRB is dummy R148, R149  
PDG is Pop R148, R149

20140520 Follow CRB0.5 and PDG0.7

Need to connect to PCH JTAC pin

20140519 Follow CRB0.5 and PDG0.7

Note :  
VCCST Power Gating (Q1) implemented : XDP\_PRESENT# need connect to Q1.G with a inverse logic.



Title	
CPU-XDP	
DWG NO	Rev
D7	X02
Date: Monday, July 27, 2015	Sheet 9 of 87

Need to check VR control power level. Level Shift?

+1POV\_VCCST R51 NI1K 5%0402 H\_CATERR#  
+1POV\_VCCST R52 NI1K 5%0402 VR\_HOT

20140516 SKL-S EDS0.75:It should be connected to VCCIO with pull-up resistor of xx

SKL S has adequate internal bias resistance on JTAG, PROC\_PRDY# to keep the devices in an idel state without the external pull resistors.

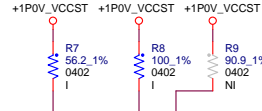
PEI-E CONFIG TABLE

CFG5	CFG6	PCI-E CONFIG
0	0	X8 X4 X4
0	1	RESERVED
1	0	X8 X8
1	1	X16

CFG	High	Low	Strap Description
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG LANE REVERSAL
3	ENABLE	DISABLE	PHYSICAL DEBUG ENABLE
4	DISABLE	ENABLE	eDP en/dis
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET_N	BIOS REQ	PEG DEFER TRAINING
8	DISABLE	ENABLE	CFG UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI AC COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYN	PMSYNC ASYN MODE
14	RESERVED		
15	RESERVED		

ALL PINS HAVE INTERNAL PULL-UPS

20140508 The resistors value of SVID follow CRB0.5 and PDG0.7



20140516 CRB0.5 add RS 33 ohm , but PDG0.7 is 20 ohm , need check Intel  
20140519 Need check with Intel about RS value . (CRB is 0 ohm , PDG0.7 is 500 ohm )  
20140519 Change net name to H\_SKT0CC#

20140520 PU EDS0.75 "Stuff R47 for Enable eDP ,unstuff R38, R1 for PCIe X16

20140520 EDS0.75 CFG[19:8]: Reserved configuration lanes.

## APU - VID.CTRL. MSIC

CPU#

BCLK#

BCLK

VIDSCLK

VIDSOUT

VIDALERT#

SELECT#

RESET#

PM\_DOWN

PM\_SYNC

PECI

CATERR#

PROC\_HOT#

THERMTRIP#

SKT0CC#

CFG[0..19]

CFG0

CFG1

CFG2

CFG3

CFG4

CFG5

CFG6

CFG7

CFG8

CFG9

CFG10

CFG11

CFG12

CFG13

CFG14

CFG15

CFG16

CFG17

CFG18

CFG19

F11

G12

H13

F13

TCK

TDI

TDO

TRST#

PRDY#

PREQ#

K9

J9

CLK24

CLK24#

CFG\_RCOMP

M11

R49

49.9 1% 0402

CFG\_RCOMP

5 OF 10

Socket\_LGA1151\_15u\_Black

XU1\_2

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

21

22

23

24

25

26

27

28

29

30

31

32

33

34

35

36

37

38

39

40

41

42

43

44

45

46

47

48

49

50

51

52

53

54

55

56

57

58

59

60

61

62

63

64

65

66

67

68

69

70

71

72

73

74

75

76

77

78

79

80

81

82

83

84

85

86

87

88

89

90

91

92

93

94

95

96

97

98

99

100

101

102

103

104

105

106

107

108

109

110

111

112

113

114

115

116

117

118

119

120

121

122

123

124

125

126

127

128

129

130

131

132

133

134

135

136

137

138

139

140

141

142

143

144

145

146

147

148

149

150

151

152

153

154

155

156

157

158

159

160

161

162

163

164

165

166

167

168

169

170

171

172

173

174

175

176

177

178

179

180

181

182

183

184

185

186

187

188

189

190

191

192

193

194

195

196

197

198

199

200

201

202

203

204

205

206

207

208

209

210

211

212

213

214

215

216

217

218

219

220

221

222

223

224

225

226

227

228

229

230

231

232

233

234

235





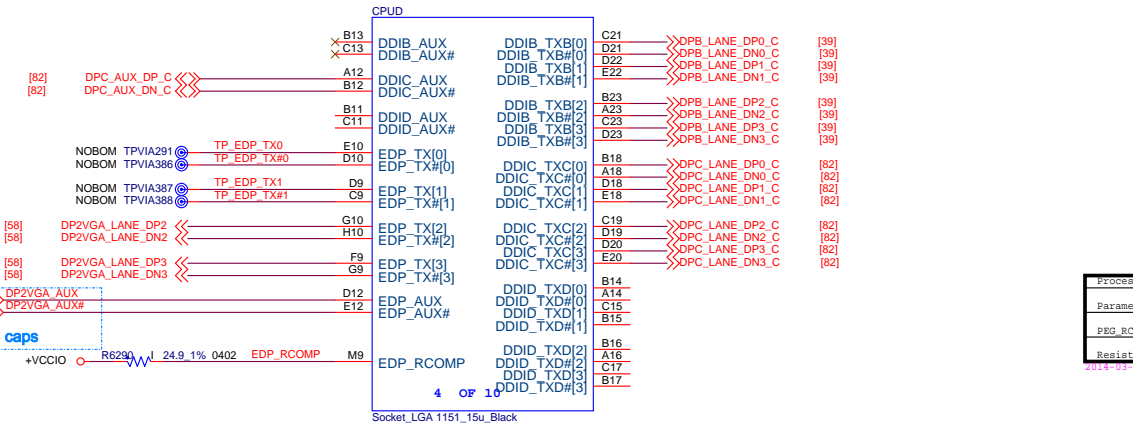
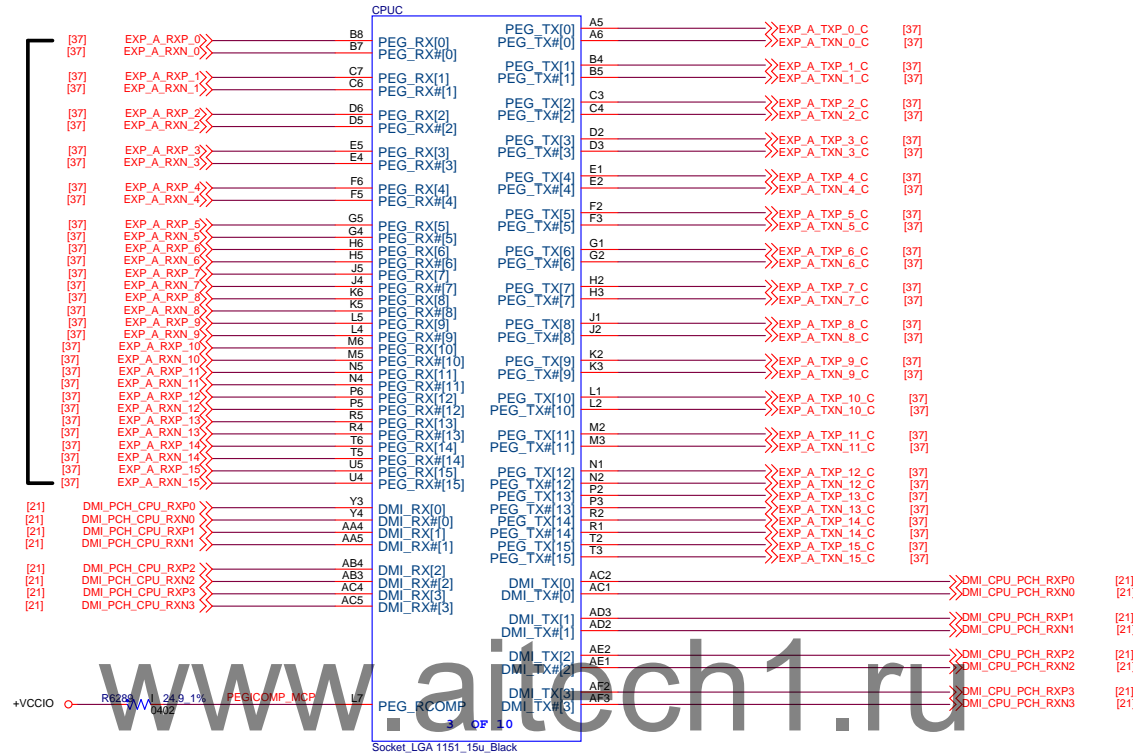
## MCP - PCIE,DMI,FDI,DDI

PEG AC Cap Value		
Gen1/Gen2	75nf-265nf	
Gen3	180nf-365nf	

PEG x16 & DMI - Refer to PDG page45  
Breakout  
MS = 10/4/4/4/10  
DSL = 10/3/3.5/3/10  
  
Main  
12/3.5/4.5/3.5/12 (Group)  
15/3.5/4.5/3.5/15 (Other)



PEG\_RCOMP:  
Trace Width = 12 mils  
Spacing = 15 mils  
Length = 400mils

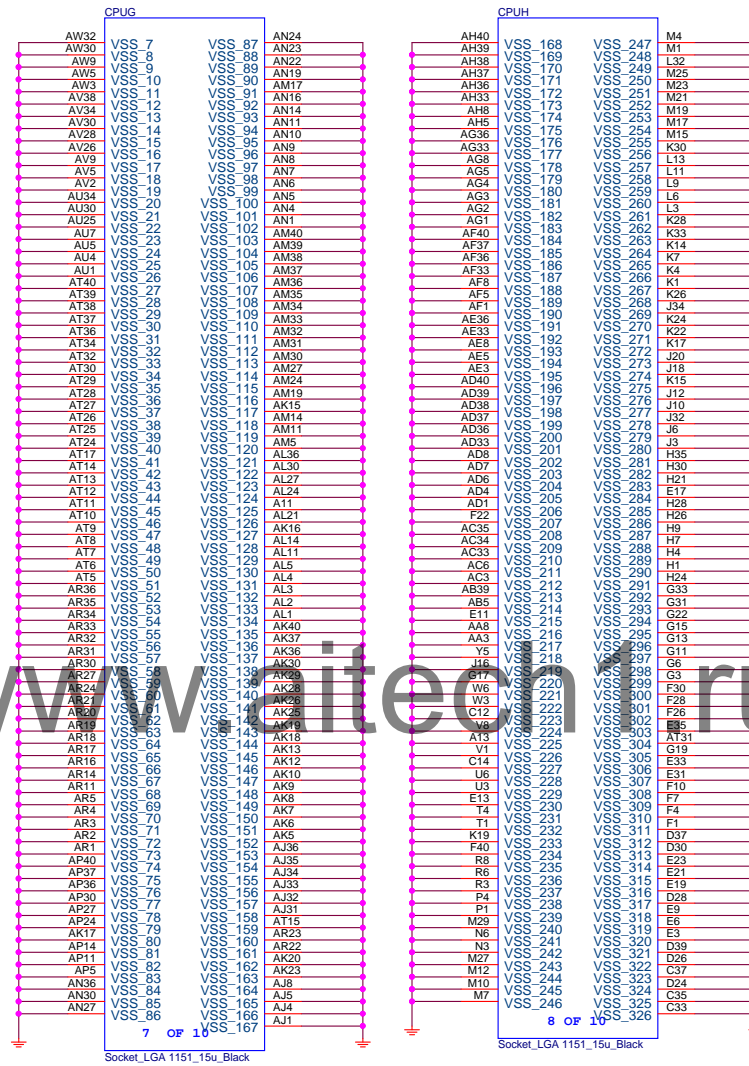


Processor PCI Express® Compensation Signal Routing Guidelines					
Parameter	Units	Trace width	Trace spacing to other signals	Routing Length	Resistance
PEG_RCOMP	mils	12	15	400	
Resistor	ohm				24.9+-1%

<b>DELL INC.</b>	
Title <b>CPU</b>	
DWG NO <b>D7</b>	Rev <b>X02</b>
Date Monday, July 27, 2015	Sheet 13 of 87







Intel PCH XDP Debug Connector

www.aitech1.ru

Project	
Spitfire	V
Scorpion	V
Toledo	V




Title	
CPU	
DWG NO	Rev
D7	X02
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru


Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru


Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru


Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru


Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru

Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	



Intel PCH XDP Debug Connector

www.aitech1.ru

Project	
Spitfire	V
Scorpion	V
Toledo	V



Title	
CPU	
DWG NO	Rev
D7	X02
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru

Project	
Spitfire	V
Scorpion	V
Toledo	V




Title	
CPU	
DWG NO	Rev
D7	X02
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru


Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru


Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru


Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru


Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru


Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru

Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	



Intel PCH XDP Debug Connector

www.aitech1.ru

Project	
Spitfire	V
Scorpion	V
Toledo	V




Title	
CPU	
DWG NO	Rev
D7	X02
Date: Monday, July 27, 2015	
Sheet	16 of 87

Intel PCH XDP Debug Connector

www.aitech1.ru


Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru


Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru


Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru


Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru

Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru

Project	
Spitfire	V
Scorpion	V
Toledo	V



Title	
CPU	
DWG NO	Rev
D7	X02
Date: Monday, July 27, 2015	
Sheet 16 of 87	

Intel PCH XDP Debug Connector

www.aitech1.ru

Project	
Spitfire	V
Scorpion	V
Toledo	V




Title	
CPU	
DWG NO	Rev
D7	X02
Date: Monday, July 27, 2015	
Sheet 16 of 87	



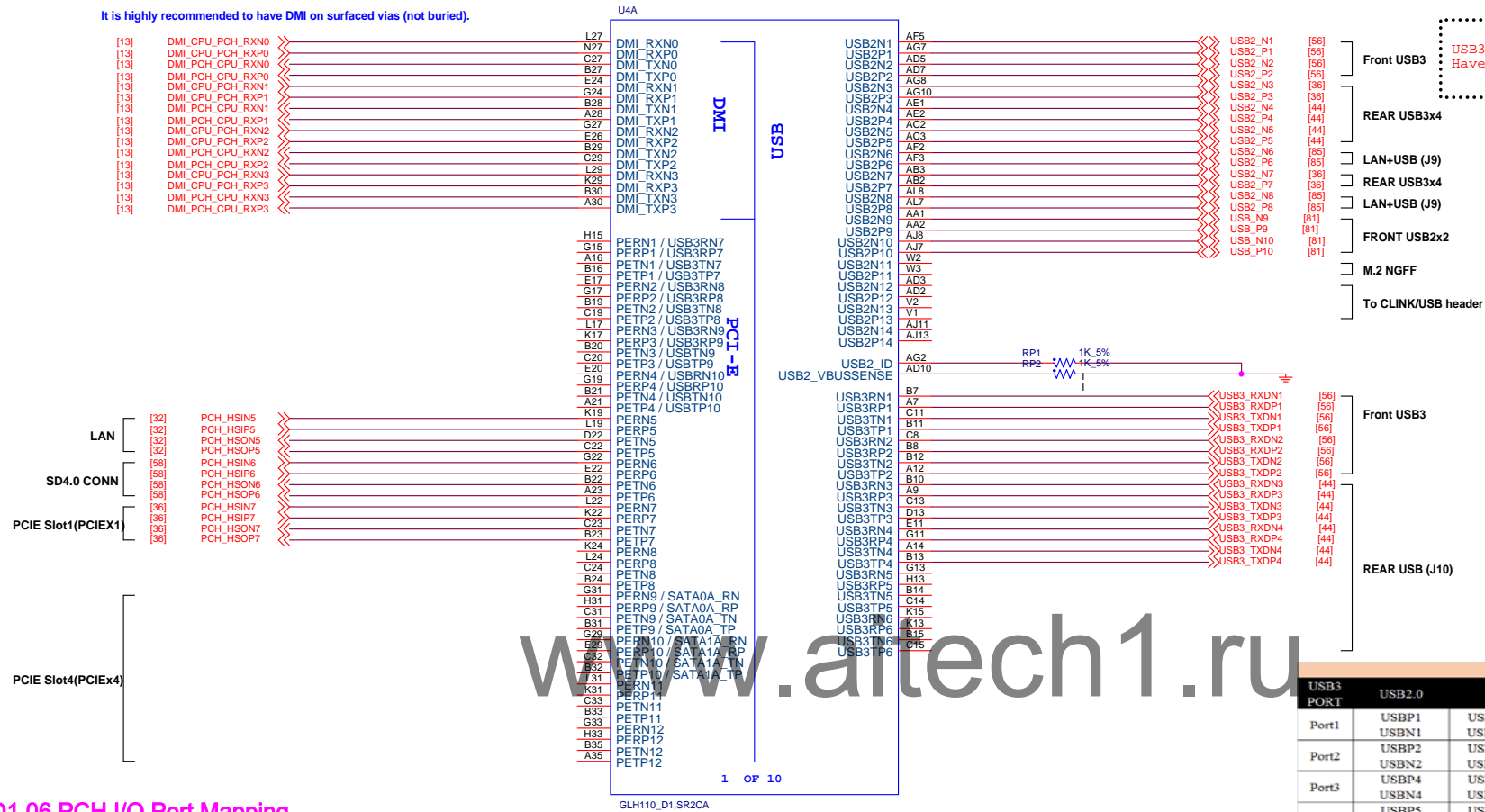
Intel PCH XDP Debug Connector

www.aitech1.ru

Project	
Spitfire	V
Scorpion	V
Toledo	V

 <b>INC.</b>	
Title	
<b>CPU</b>	
DWG NO	Rev
<b>D7</b>	<b>X02</b>
Date: Monday, July 27, 2015	
Sheet 16 of 87	

It is highly recommended to have DMI on surfaced vias (not buried).



## ARD1.06 PCH I/O Port Mapping

	Intel	3 Series PCB, H110		7/9 Series PCB, Q170	
Port#	Sunrise-Point	Interface	Device	Interface	Device
1	USB3#1	USB3	Front USB3 conn.	USB3	Front USB3 conn.
2	USB3#2	USB3	Front USB3 conn.	USB3	Front USB3 conn.
3	USB3#3	USB3	Rear USB3 conn.	USB3	Rear USB3 conn.
4	USB3#4	USB3	Rear USB3 conn.	USB3	Rear USB3 conn.
5	USB3#5			USB3	Rear USB3 conn.
6	USB3#6			USB3	Rear USB3 conn.
7	USB3#7/PCIE#1				
8	USB3#8/PCIE#2				
9	USB3#9/PCIE#3				
10	USB3#10/PCIE#4/GbE				
11	PCIE#5/GbE	PCle	NIC	GbE	Intel NIC
12	PCIE#6	PCle	SD 4.0 CR	PCle	SD 4.0 CR
13	PCIE#7	PCle	PCle slot 1 (x1)		
14	PCIE#8	PCle	M.2 WLAN*	PCle	M.2 WLAN*
15	PCIE#9/SATA#0/GbE			PCle	PCle slot 1 (x4)
16	PCIE#10/SATA#1			PCle	PCle slot 1 (x4)
17	PCIE#11			PCle	PCle slot 1 (x4)
18	PCIE#12/GbE			PCle	PCle slot 1 (x4)
19	PCIE#13/SATA#0/GbE	SATA	HDD1	SATA	HDD1
20	PCIE#14/SATA#1	SATA	HDD2/ODD	SATA	HDD2/ODD
21	PCIE#15/SATA#2			SATA	HDD3
22	PCIE#16/SATA#3	SATA	M.2 SSD*		
23	PCIE#17/SATA#4			SATA/PCle	M.2, SSD SATA/PCle lane 1
24	PCIE#18/SATA#5			SATA/PCle	M.2, SSD PCle lane 2
25	PCIE#19			PCle	M.2, SSD PCle lane 3
26	PCIE#20			PCle	M.2, SSD PCle lane 4

USB Pin Assignment						
USB2 Port	Pin Name	Pin Type	USB OC Port	Y/N	Note	Location
1	USB2N1/P1	IN/OUT	USB_OC0_R_N	Y	Front USB3.0	USB3F2 port1
2	USB2N2/P2	IN/OUT		Y	Front USB3.0	USB3F2 port2
3	USB2N4/P4	IN/OUT	USB_OC1_R_N	Y	Rear USB 3.0x4 Down	USB3R1 port 1
4	USB2N5/P5	IN/OUT		Y	Rear USB 3.0x4 Down	USB3R1 port 2
5	USB2N7/P7	IN/OUT	USB_OC2_R_N	Y	Rear USB 3.0x4 up	USB3R1 port 3
6	USB2N3/P3	IN/OUT		Y	Rear USB 3.0x4 up	USB3R1 port 4
7	USB2N8/P8	IN/OUT	USB_OC3_R_N	Y	RJ45+Rear USB2.0 W Smart pwr on	RJ45 USB port1
8	USB2N6/P6	IN/OUT		Y	RJ45+Rear USB2.0 W Smart pwr on	RJ45 USB port2
9	USB2N9/P9	IN/OUT	USB_OC4_R_N	Y	Front USB2.0 W/O CHARGER	USB2F1 port1
10	USB2N10/P10	IN/OUT	USB_OC6_R_N	Y	Front USB2.0 W CHARGER	USB2F1 port2
11	USB2N11/P11	IN/OUT	N/A	N	N/A	N/A
12	USB2N12/P12	IN/OUT	USB_OC5_R_N	Y	CLINK/USB HEADER	CLINK1 port1
13	USB2N13/P13	IN/OUT		Y	CLINK/USB HEADER	CLINK1 port2
14	USB2N14/P14	IN/OUT	N/A	N	N/A	N/A

FXN USB Port Mapping				
USB3 PORT	USB2.0	USB3.0	Function	Note
Port1	USBP1	USB3Tp1 USB3Tn1	Front USB3.0	
	USBN1	USB3Rn1 USB3Rp1		
Port2	USBP2	USB3Tp2 USB3Tn2	Rear USB3X4 down	
	USBN2	USB3Rn2 USB3Rp2		
Port3	USBP4	USB3Tp3 USB3Tn3	Rear USB3X4 up	SFF3: CLINK/BT
	USBN4	USB3Rn3 USB3Rp3		
Port4	USBP5	USB3Tp4 USB3Tn4	Rear USB3X4 down	
	USBN5	USB3Rn4 USB3Rp4		
Port5	USBP7	USB3Tp5 USB3Tn5	Rear USB3X4 up	SFF3: CLINK/BT
	USBN7	USB3Rn5 USB3Rp5		
Port6	USBP3	USB3Tp6 USB3Tn6	Rear USB3X4 up	SFF3: CLINK/BT
	USBN3	USB3Rn6 USB3Rp6		

Title

PCH

DWG NO

D7

Rev

X02

Date:

Monday, July 27, 2015

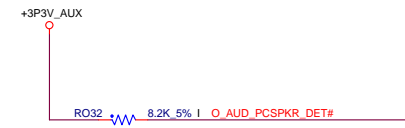
Sheet

21

of

87

ROUTE NOTE:  
MINIMIZE STUB TO PULL UP RES for AR44,AR11



[29,36,37]  
[29,36,37]  
[26]  
SMBCLK  
SMBDATA  
PCH\_STRAP\_TL5



[26]  
[29]  
[29]  
PCH\_STRAP\_ESPLEN  
SML1CLK\_PCH  
SML1DATA\_PCH



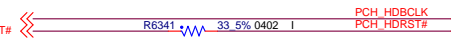
NOBOM  
NOBOM  
TPVIA421  
TPVIA422



[29] RING#



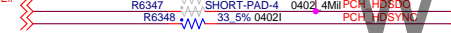
[34] AUD\_BITCLK  
[34,35] AUD\_LINK\_RESET#



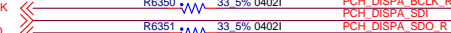
[34] AUD\_LINK\_SDIO



[28] FLASH\_OVERRIDE#  
[34] RSDATA\_OUT  
[34] AUD\_SYNC



[10] PCH\_DISPA\_BCLK  
[11] PCH\_DISPA\_SDI  
[11] PCH\_DISPA\_SDO



[10] CL\_CLK\_WLAN  
[36] CL\_DATA\_WLAN  
[36] CL\_RST\_WLAN#



AL39  
AN36  
AN38  
AN41  
AM44  
AJ33  
AM43  
AN42  
AL42  
AL44  
AL36  
AL35  
AJ39  
AK45  
AK44  
AL43  
AJ43  
AJ42  
AJ38  
AJ35  
AG44  
AH44  
AH43  
AJ44

TPVIA423  
O\_AUD\_PCSPKR\_DET#  
O\_FP\_CBL\_DET#

TPVIA424  
NOBOM

TPVIA425  
TPVIA426  
NOBOM  
NOBOM

AY5  
<<H\_TRST#\_R [9]

Refer to SKL PCH-H EDS 0.5  
JTAG\_TCK/TMS/TDI/TDO/JTAGX have internal Pdor PU  
AN3 PCH\_JTAG\_TCK  
AP2 PCH\_JTAG\_TDI  
AP2 F\_PCH\_JTAG\_TMS  
AP3 XDP\_PCH\_JTAGX  
AP1 F\_PCH\_JTAG\_TDO  
PCH\_JTAG\_TCK [52]  
F\_PCH\_JTAG\_TDI [52]  
F\_PCH\_JTAG\_TMS [52]  
H\_TCK [9,10]  
F\_PCH\_JTAG\_TDO [52]

AT4  
AT3  
PRDY\_N  
PREQ\_N

AK1 H\_CPU\_PCH\_TRIGGER\_OUT  
AL2 H\_CPU\_PCH\_TRIGGER\_IN

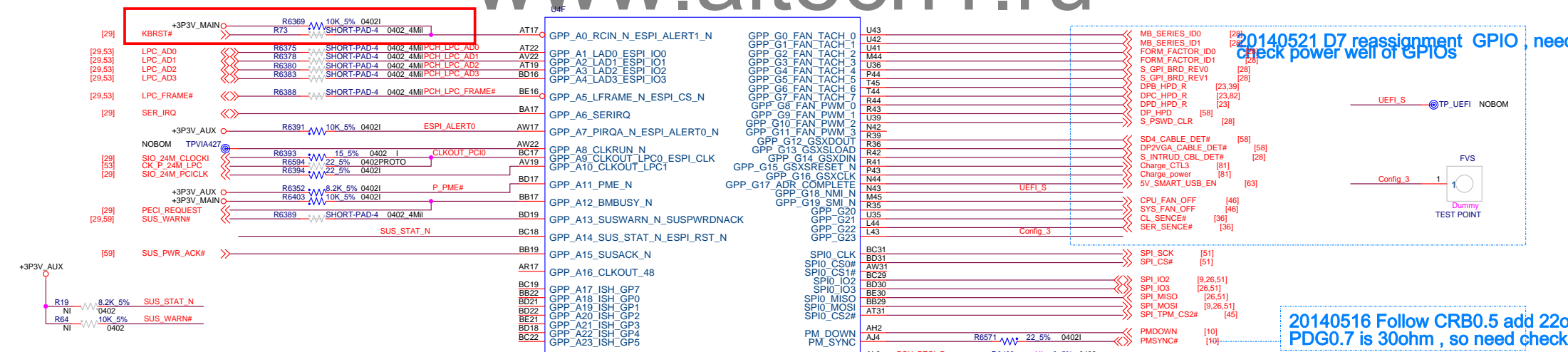
20140519 Follow CRB0.5 and PDG0.7  
Need check Debug port PDG

F\_PCH\_JTAG\_TMS RP8 NI0.5% 0402 H\_TMS [9,10]  
F\_PCH\_JTAG\_TDI RP10 NI0.5% 0402 H\_TDI [9,10]  
F\_PCH\_JTAG\_TDO RP11 NI0.5% 0402 H\_TDO [9,10]

Title <b>PCH</b>	
DWG NO <b>D7</b>	Rev <b>X02</b>
Date: Monday, July 27, 2015 Sheet 22 of 87	



www.aitech1.ru



**EPISI Interface**  
ESPI\_IO[3:0]  
ESPI\_CLK  
ESPI\_CS#  
ESPI\_RESET#

LPC  
RES place close to PCH within 2inch  
P1V8\_P3V3\_PCH\_GPPA  
LPC : 3.3V  
ESPI : 1.8V

When eSPI enabled,  
all group A pins  
operate at 1.8v

When LPC enabled,  
all group A pins  
operate at 3.3v

**DELL INC.**

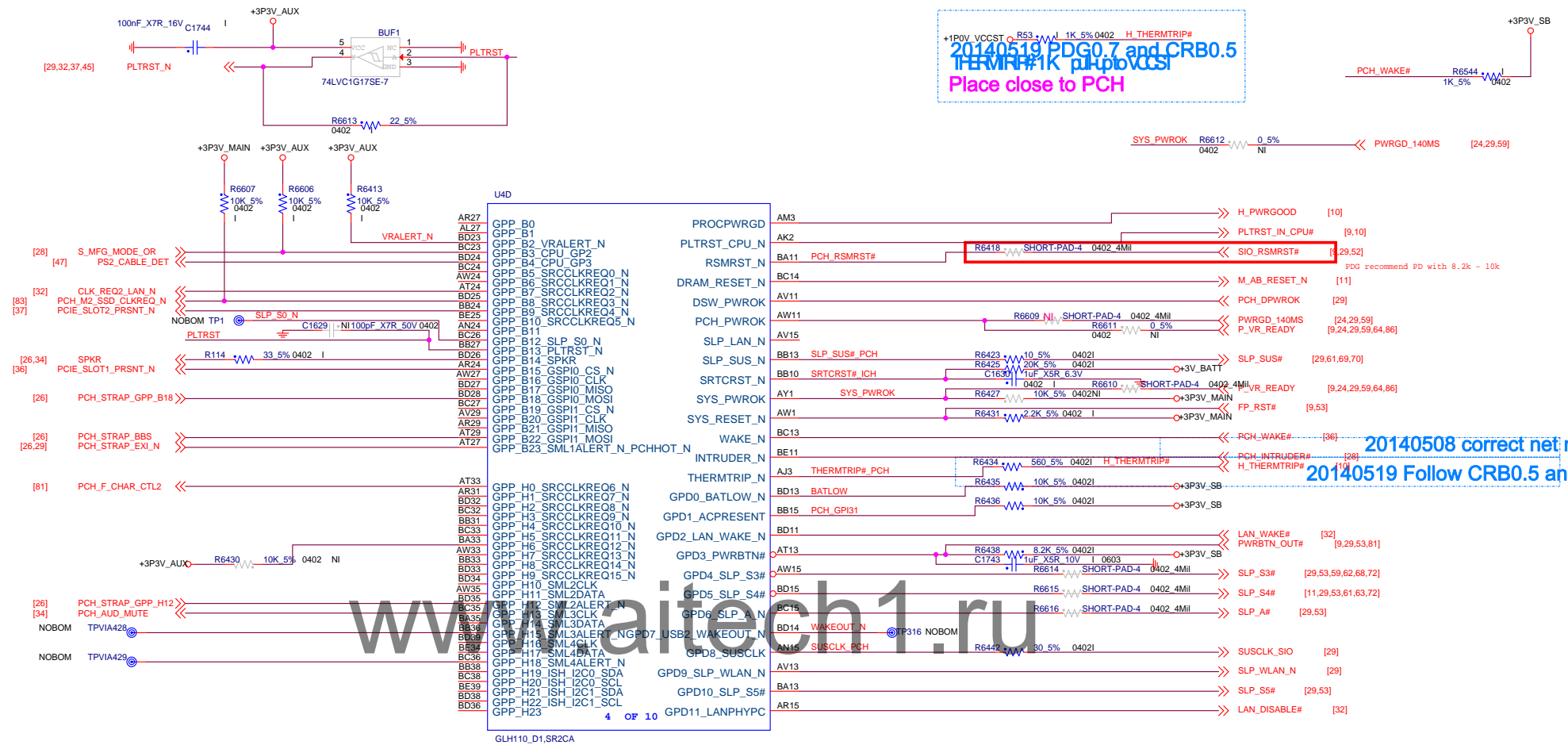
Title: **PCH**

DWG NO: **D7**

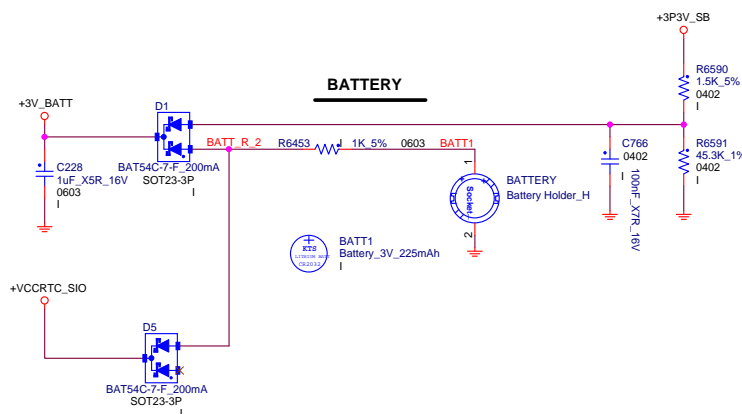
Rev: **X02**

Date: Monday, July 27, 2015 Sheet 23 of 87

20140516 Folow CRB0.5

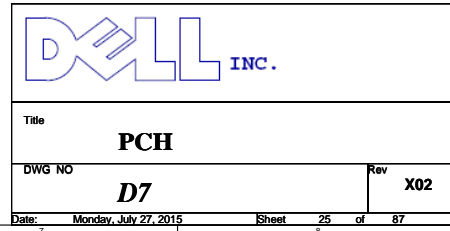


www.aiotech1.ru

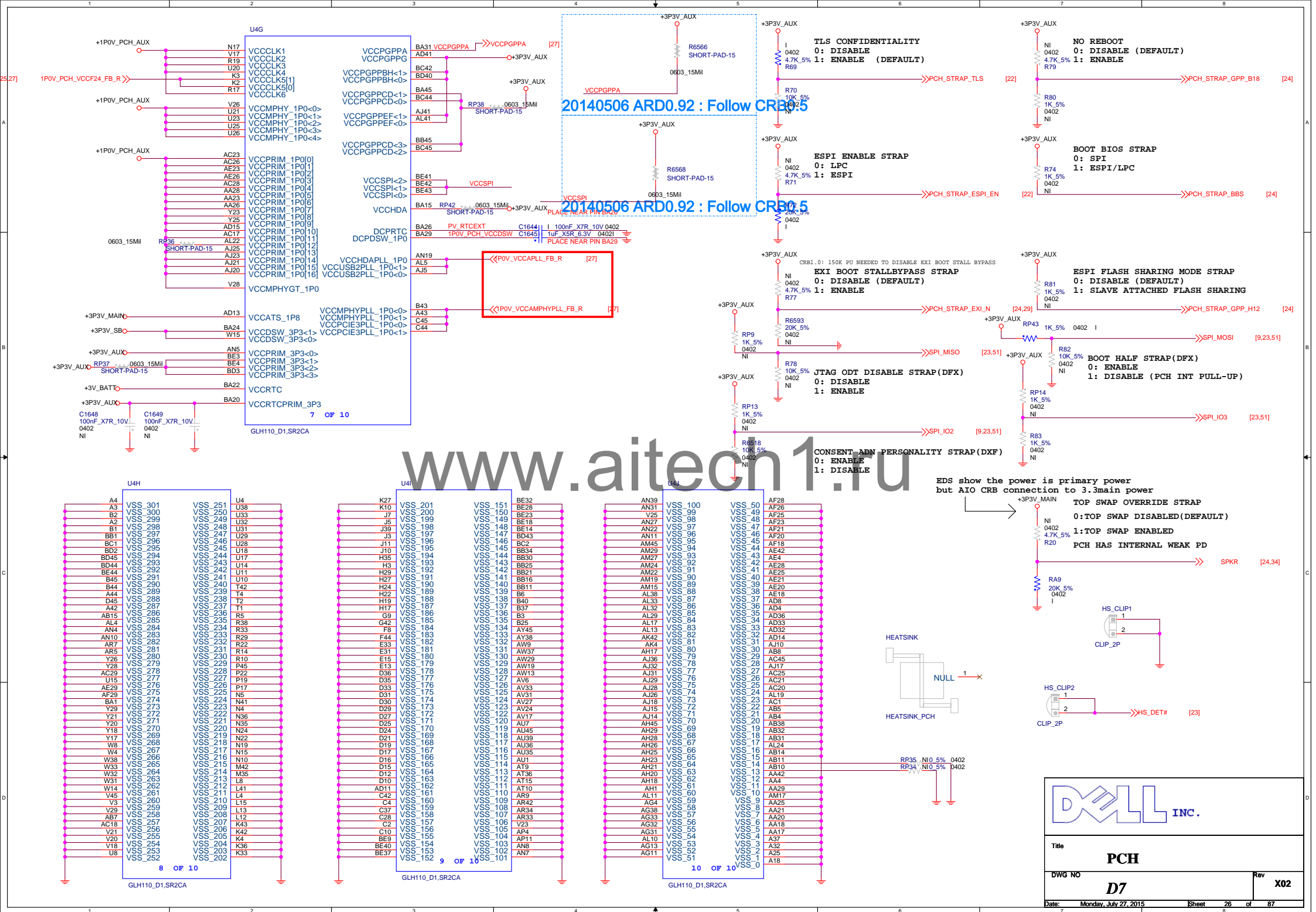


Title <b>PCH</b>	
DWG NO <b>D7</b>	Rev <b>X02</b>
Date: Monday, July 27, 2015 Sheet 24 of 87	


www.aitech1.ru





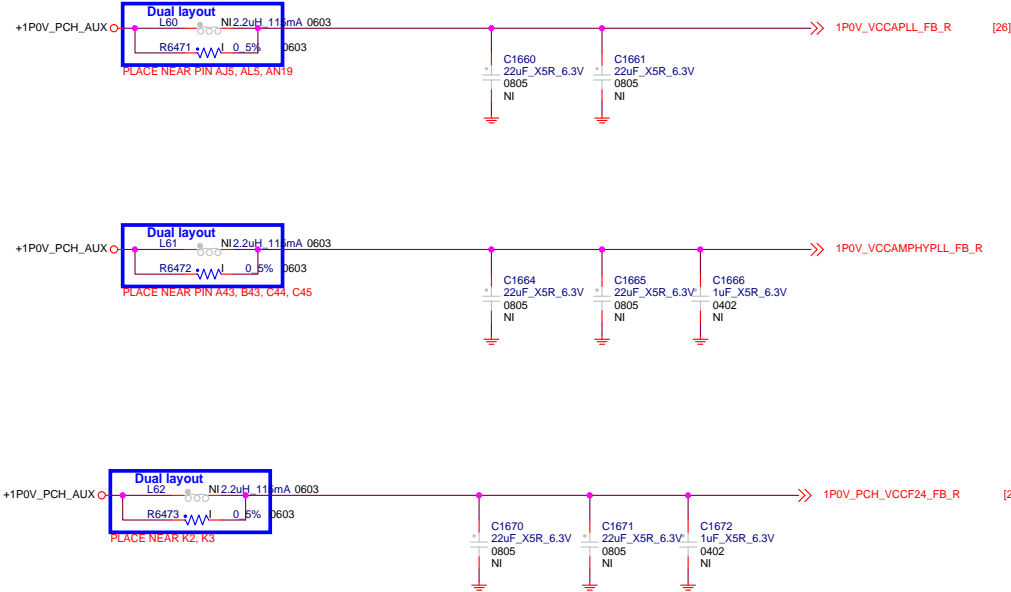


www.aitech1.ru

	
Title <b>PCH</b>	
DWG NO <b>D7</b>	Rev <b>X02</b>
Date: Monday, July 27, 2015	
Sheet 26 of 87	

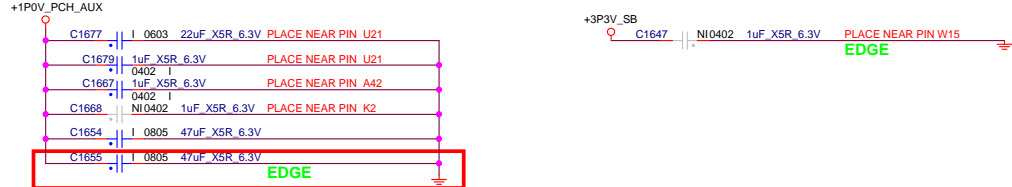
SKYLAKE Decoupling & filter

FILTER



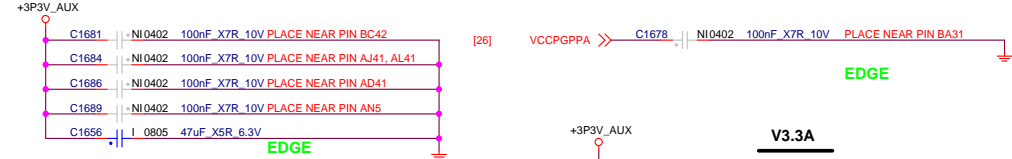
V1.0A

V3.3 DSW



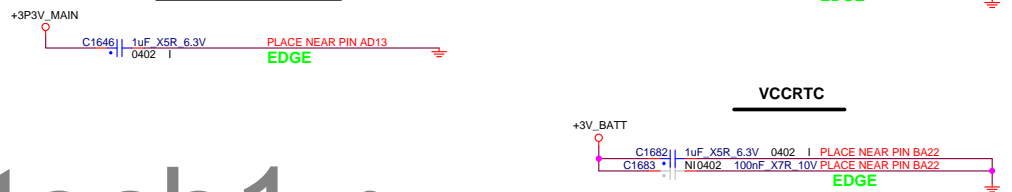
V1.8A / V3.3A

VccPGPPA

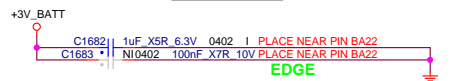


V1.8A / V1.8S / V3.3S

V3.3A



VCCRTC

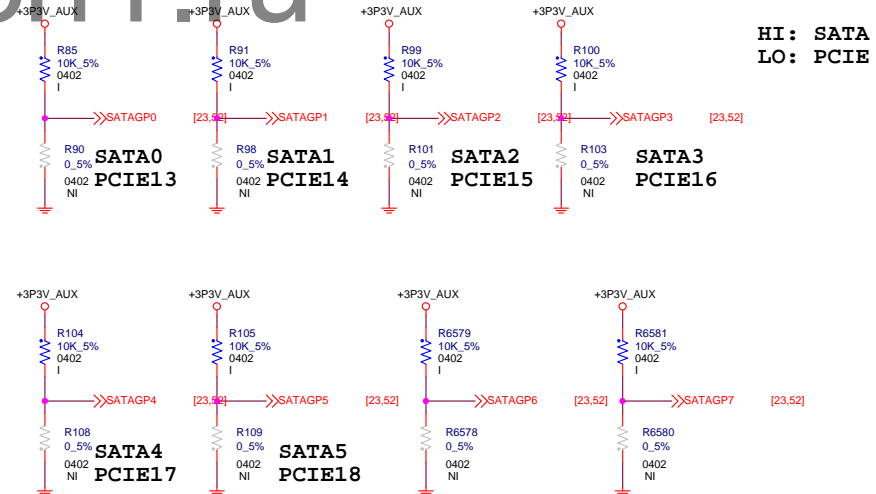


Power Plane Isolation

Need to update for SLK

Voltage	Interface	PCH Pins sharing power rail
VCC_PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	T19, T20, P22, P23, P25, P26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14 W14 AB2
	SSC	T16, V16 AA16, W16
PCH 3.3V Standby	USB2	AF19, AF20, AF22, AF23, AP22
	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
	AZALIA	AW26
	USB3	P20
PCH 3.3V	RTC	AP35
	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
	HVCNOS	AG1
	PCIe	AV3, AW3
	Core	U30, W30
	Fuse	AF26

www.aitech1.ru



HI: SATA  
LO: PCIE

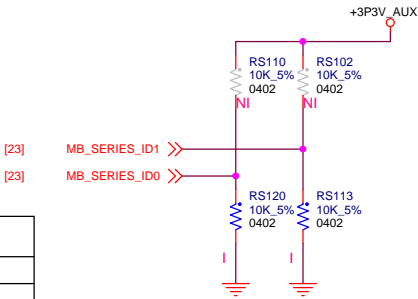


Title	
PCH	
DWG NO	Rev
D7	X02
Date: Monday, July 27, 2015	Sheet 27 of 87



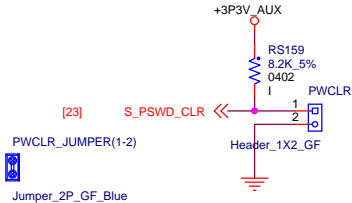
MB series ID

ID1	ID0	Type
0	0	SFF3
0	1	SFF5
1	0	SFF7
1	1	Farallon



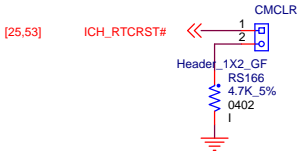
Clear Password

PASSWORD	SHORT : DEFAULT
	OPEN : CLEAR PASSWORD



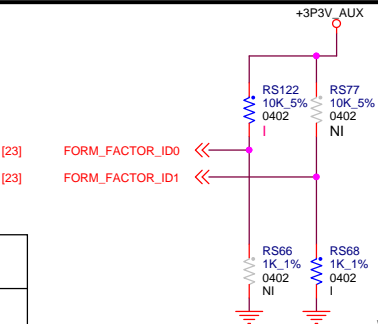
CLR\_CMOS

CMOS	SHORT : CLEAR CMOS
	OPEN : DEFAULT

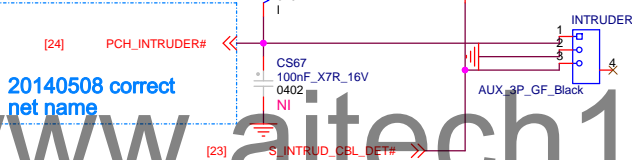


Form Factor ID

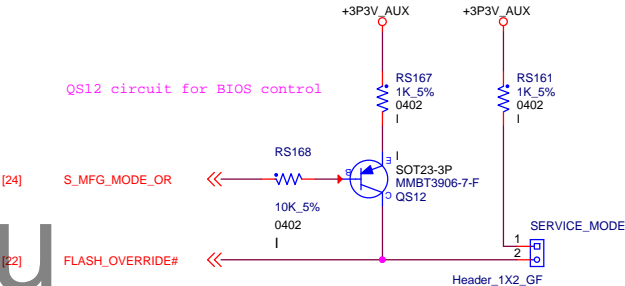
ID1	ID0	Type
1	1	MT
1	0	CT
0	1	SFF
0	0	Micro



Chassis Intruder

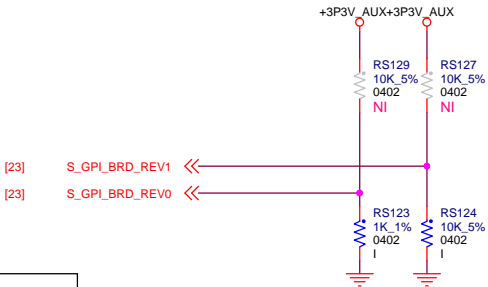


ME Disable (Flash override)



BOARD ID

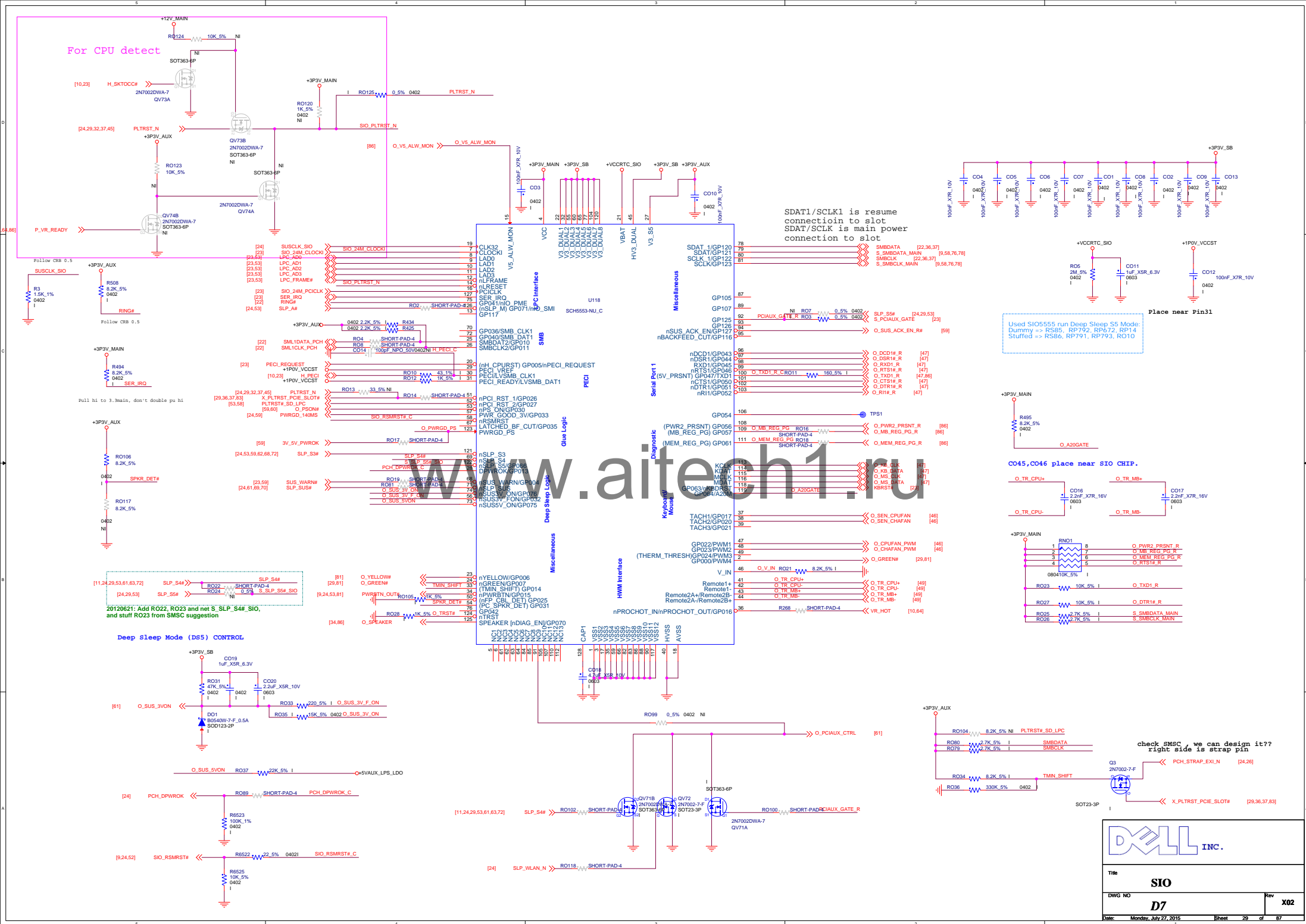
ID1	ID0	Type
1	1	X02
1	0	X01
0	1	X00
0	0	B00/A00

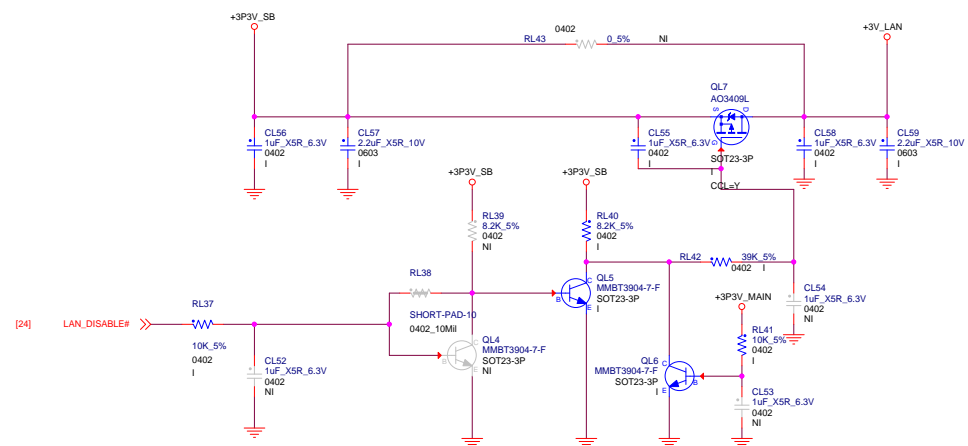


BEEP

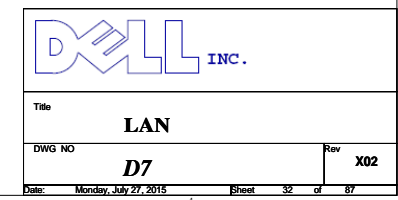
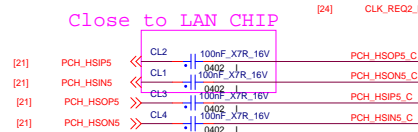


Title		PCH	
DWG NO		D7	
Date: Monday, July 27, 2015		Sheet 28 of 87	





The schematic diagram illustrates the power and crystal sections of the circuit. The power section features a +3P3V MAIN supply connected to a 1K 5% resistor (RL34) and a 15K 5% resistor (RL35) in series, with a 0402 capacitor (I) connected to ground. The crystal section shows a 25MHz crystal connected to XTAL\_OUT and XTAL\_IN, with 27pF NPO 50V capacitors (CL36 and CL37) connected to ground.



20140507 Reserved +3.3V for AVDD2 for cost saving, but need REALTEK final report.

Layout: Close to codec

20140514 Realtek suggestion

Layout: Close to pin1

20140516 Realtek suggestion

there is a PCBEEP input detect circuit (inside the codec) to power up Class-D amplifier function requires this voltage divider circuit to get over TV input voltage.

Layout: Close to pin9

20140507 For TI chip 1.5V, this is template solution waiting CE for final solution suggestion

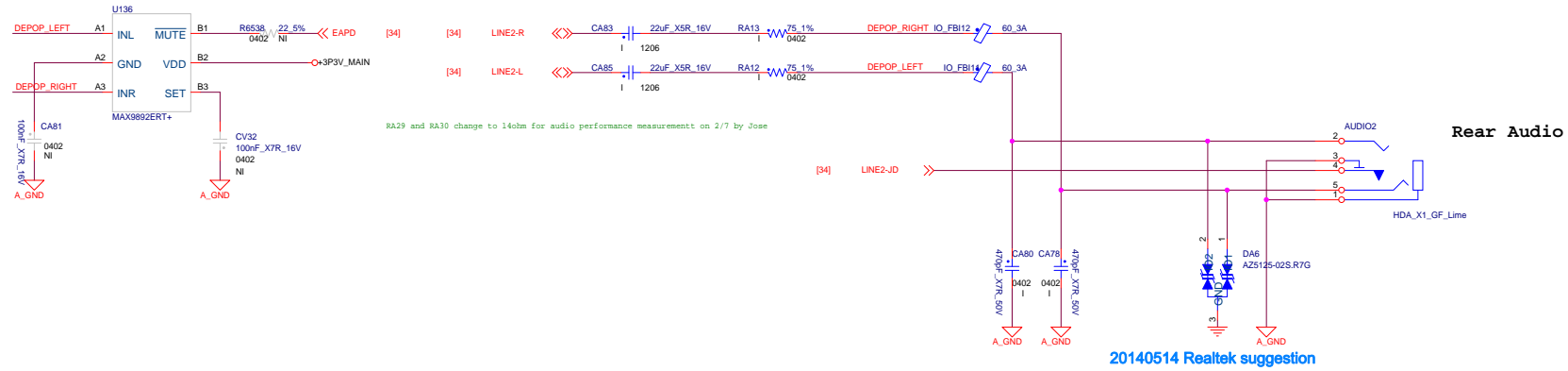
201405012 Follow DC use 5325, waiting confirm CE for final solution suggestion

$$V_{out} = 0.8 * (1 + RK33 / RK35) = 1.52V$$

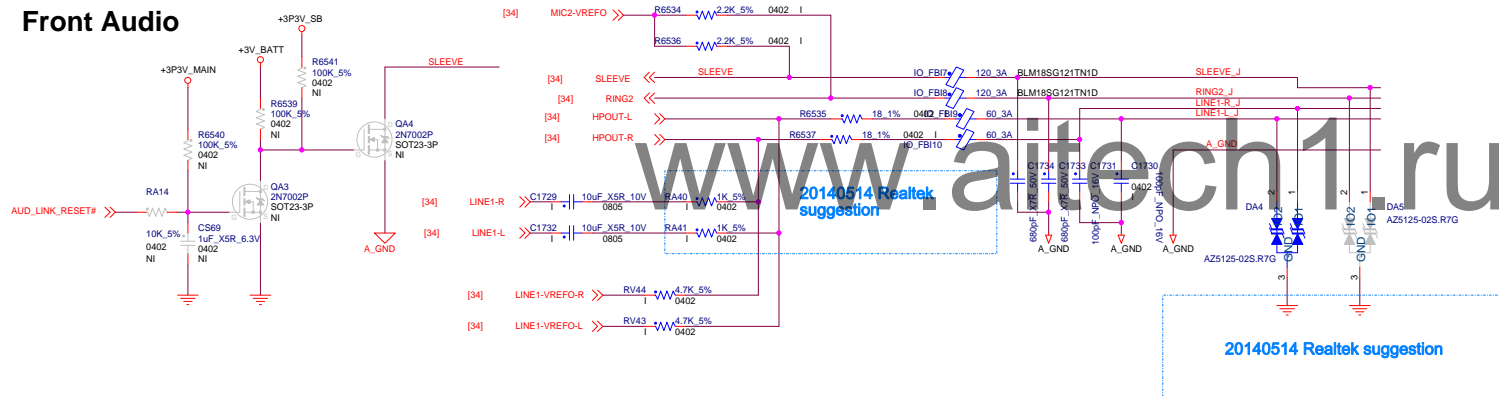
20140514 Realtek suggestion: If mobile-HDA link used 1.8V power domain, please reserve a level shift circuit.

www.aitech1.ru

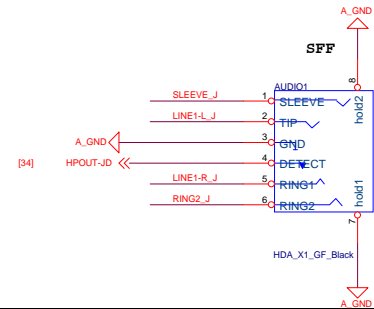
## Rear Audio Jack



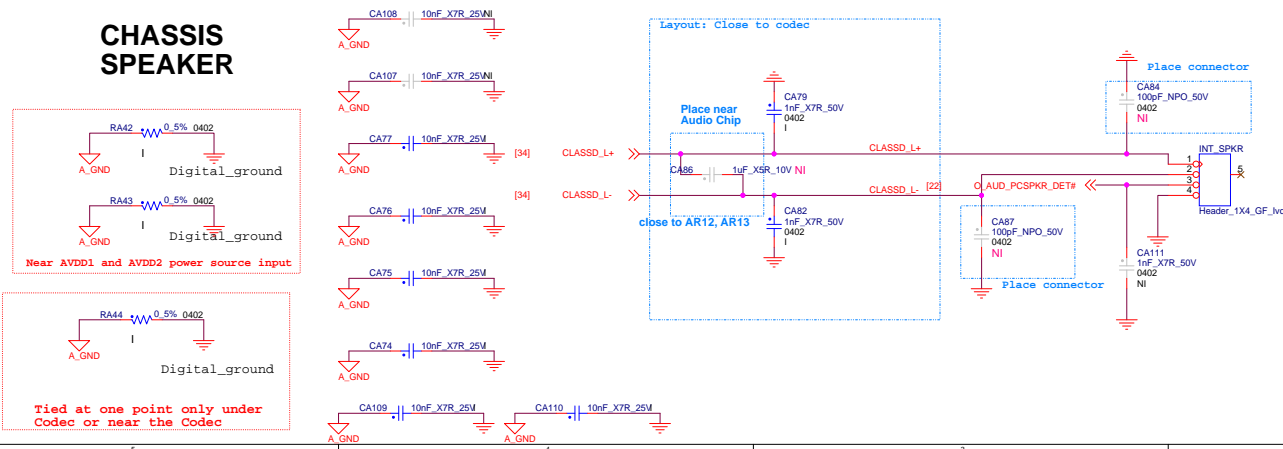
## Front Audio



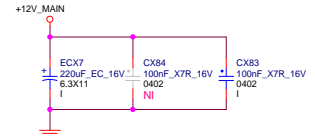
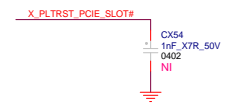
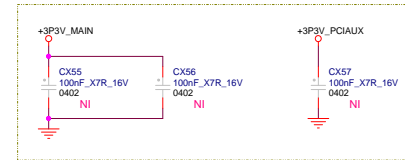
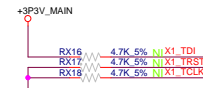
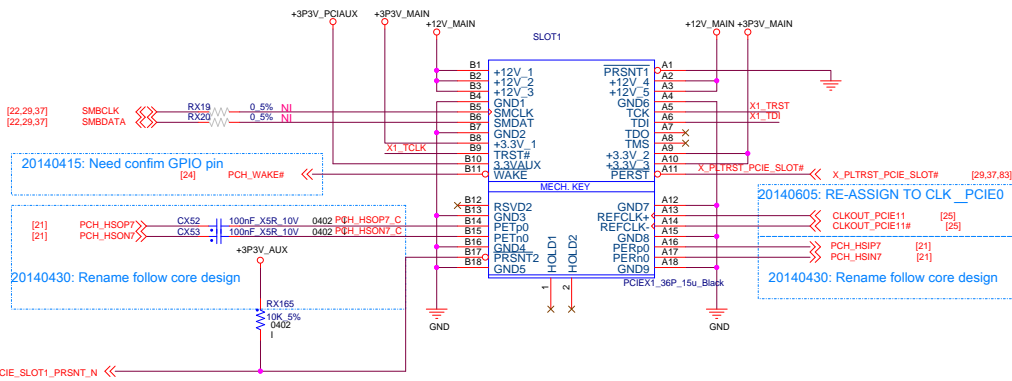
## Front Panel



## CHASSIS SPEAKER



Title		
AUDIO		
DWG NO	D7	Rev X02
Date	Monday, July 27, 2015	Sheet 35 of 87

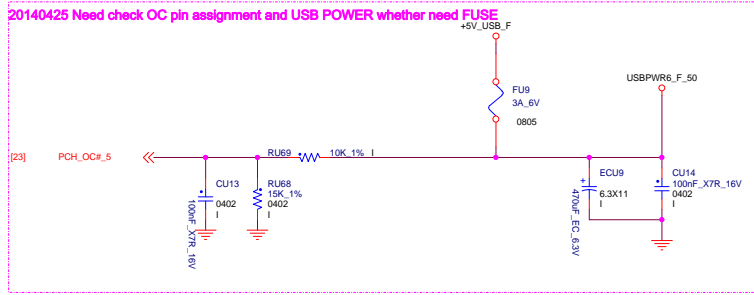
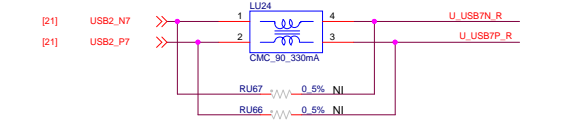
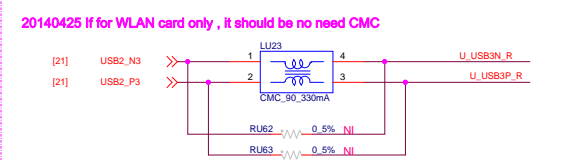
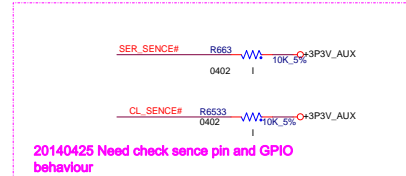
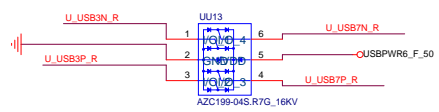
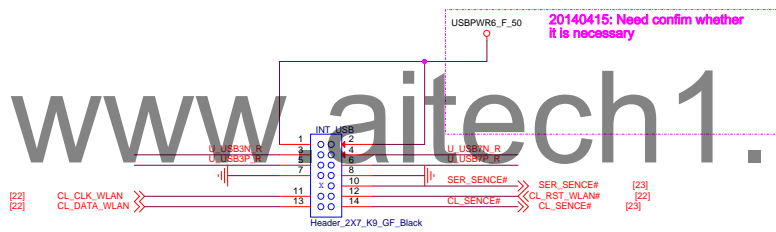


ARD 0.9 :Header populated on 7/9 series only  
Provides vPro and BT support from Intel wireless Add-in-Card  
USB and CLINK signals passed on cable from motherboard to Add-in-Card  
Compatible with standard USB 2.0 headers and cables

14 pin non shrouded header 0.1 pin spacing,  
Pin 14 allows sense of the CLINK/BT cable ,  
Add-in-Card does not use +5V\_USB or USB2\* (second port) signals

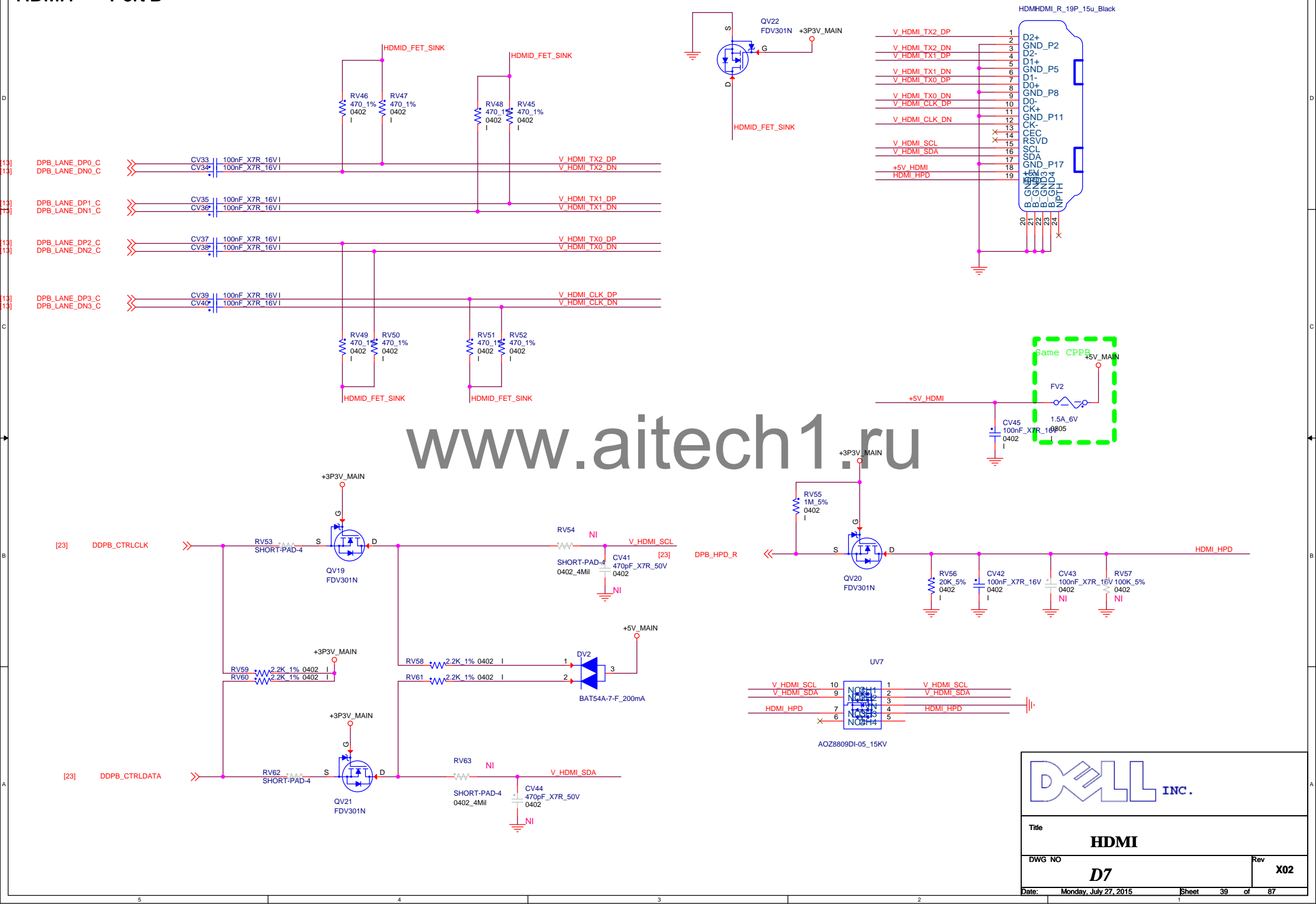
14 pin USB/CLINK Header			
+ 5V_USB	1	2	+ 5V_USB
USB1N	3	4	USB2N
USB1P	5	6	USB2P
GND	7	8	GND
Key (no pin)	9	10	SER_SENSE
CLINK_CLK	11	12	CLINK_RST
CLINK_DAT	13	14	CL_SENSE

www.aitech1.ru






HDMI1 --> Port B



www.aitech1.ru

**INC.**

Title

**HDMI**

DWG NO

**D7**

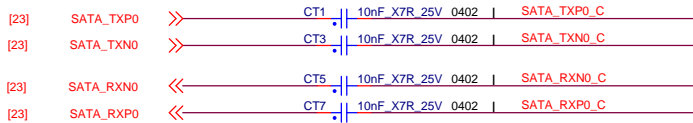
Rev

**X02**

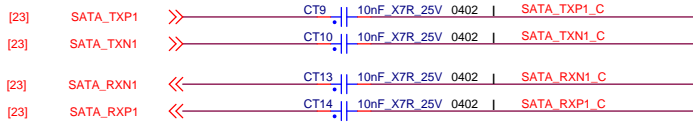
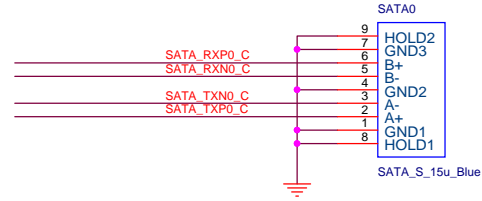
Date: Monday, July 27, 2015

Sheet 39 of 87

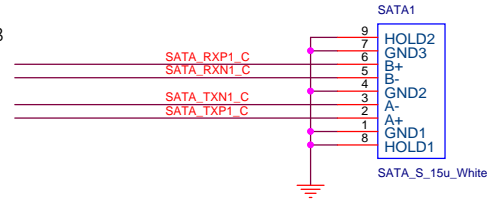




Blue SATA3

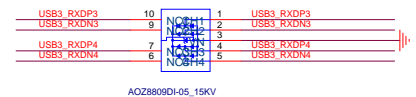
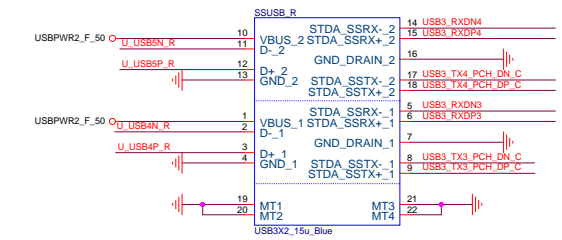
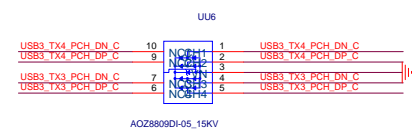
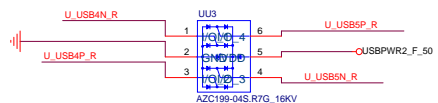
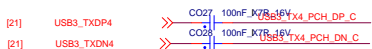
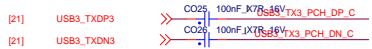
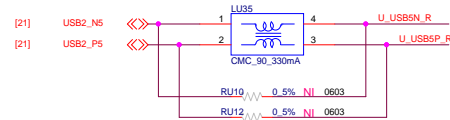
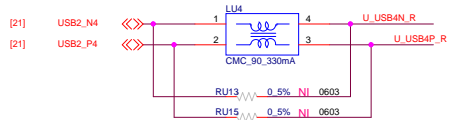


white ODD SATA3



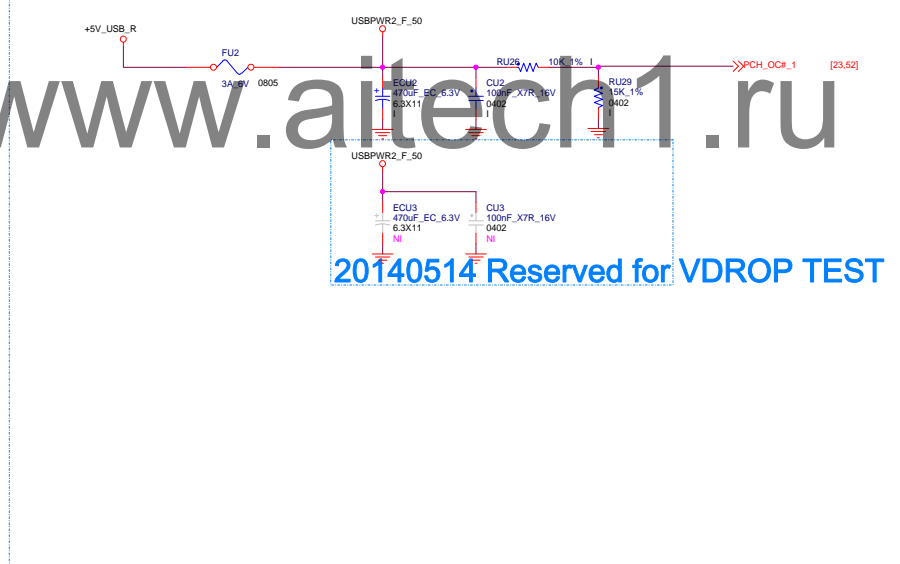
www.aitech1.ru





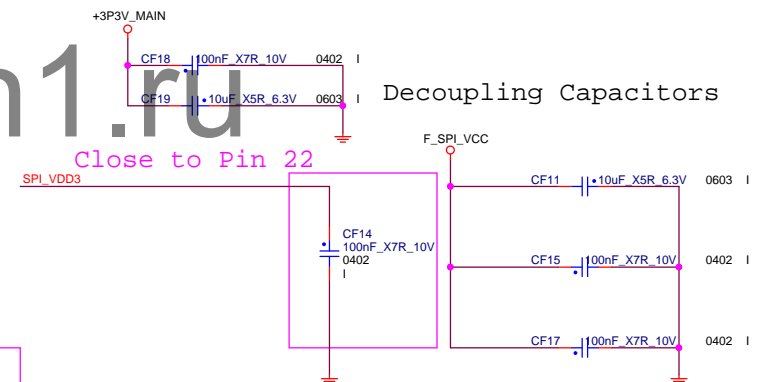
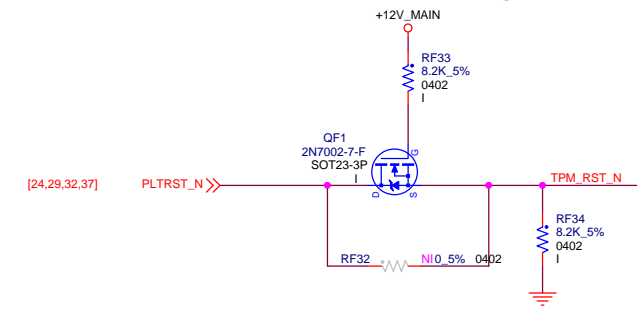
20140505 ARD0.92: Each pair of USB ports will be current limited to 2.5A

www.aitech1.ru



20140514 Reserved for VDROP TEST

HW Low Power Mode	RF62	RF63	RF60
Support	Un-stuff	Stuff	Stuff
Not support	Stuff	Un-stuff	Un-stuff



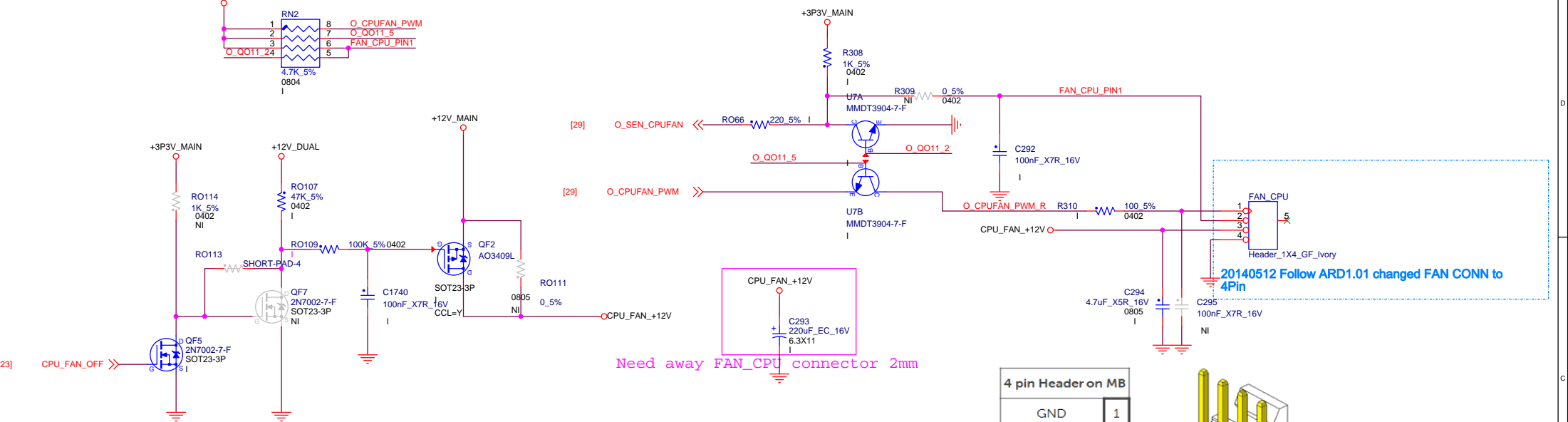
NOTE:

- Place 0.1 uF capacitors as close as possible to the device power pins.
- CF17 is required only for the NPCT620/650.

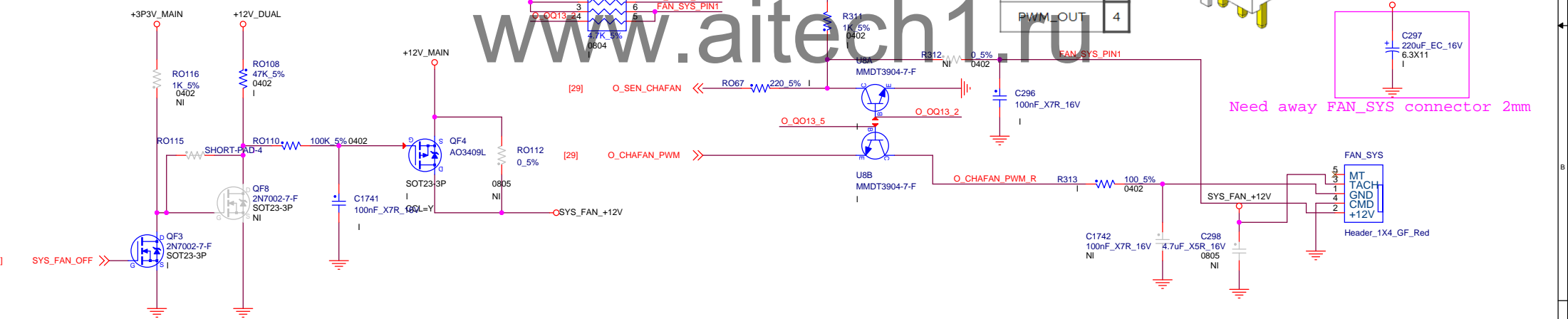


Title		<b>TPM</b>	
DWG NO		<b>D7</b>	Rev <b>X02</b>
Date:	Monday, July 27, 2015	Sheet	45 of 87

CPU Fan



SYS Fan



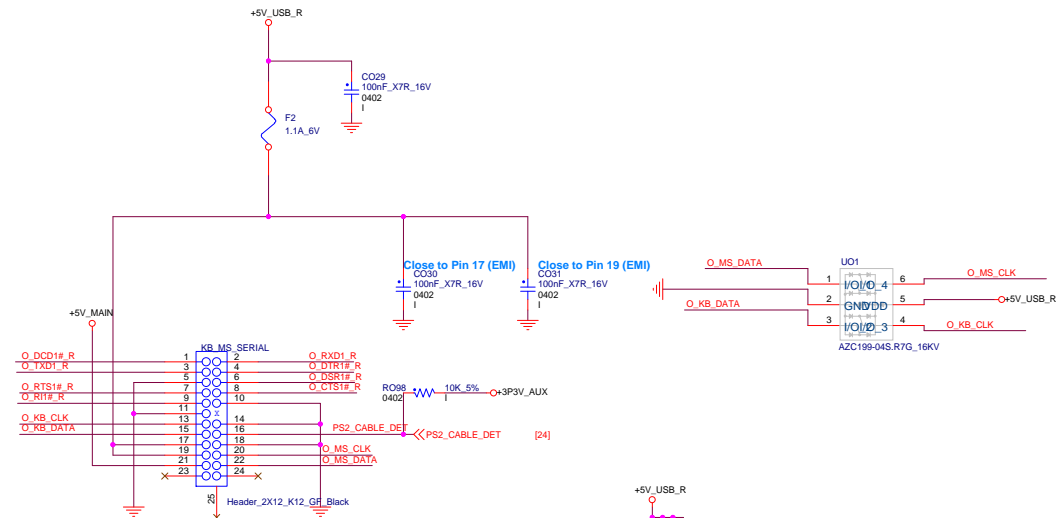
LABEL



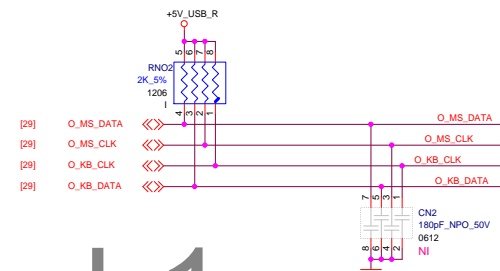
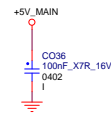
Serial Port 1

KB/MS

[29] O\_R1#\_R << O\_R1#\_R  
[29] O\_CTS1#\_R << O\_CTS1#\_R  
[29] O\_DSR1#\_R << O\_DSR1#\_R  
[29] O\_RTS1#\_R << O\_RTS1#\_R  
[29] O\_DTR1#\_R << O\_DTR1#\_R  
[29] O\_TXD1#\_R << O\_TXD1#\_R  
[29,86] O\_RXD1#\_R << O\_RXD1#\_R  
[29] O\_DCD1#\_R << O\_DCD1#\_R

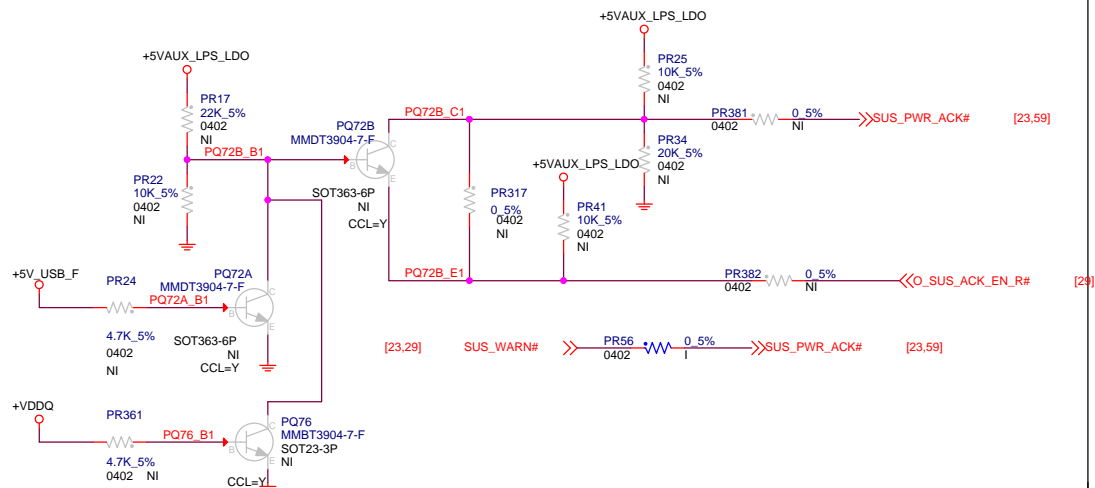


20140512 Need check pin define

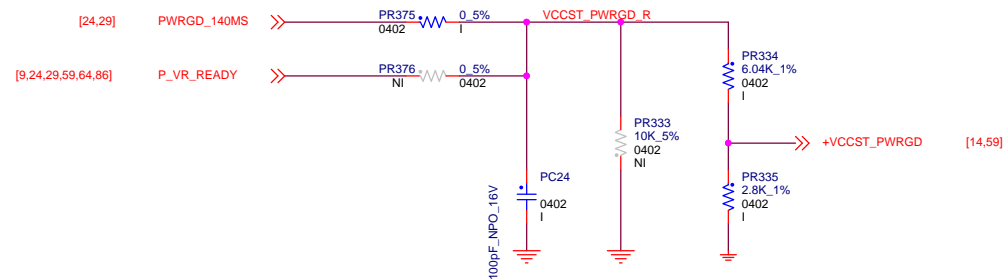


www.aitech1.ru

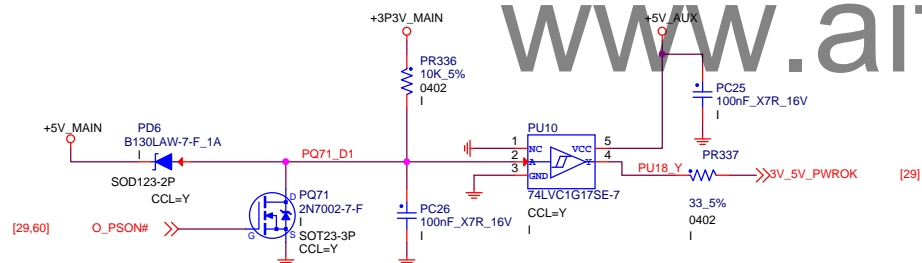
# Power Sequence



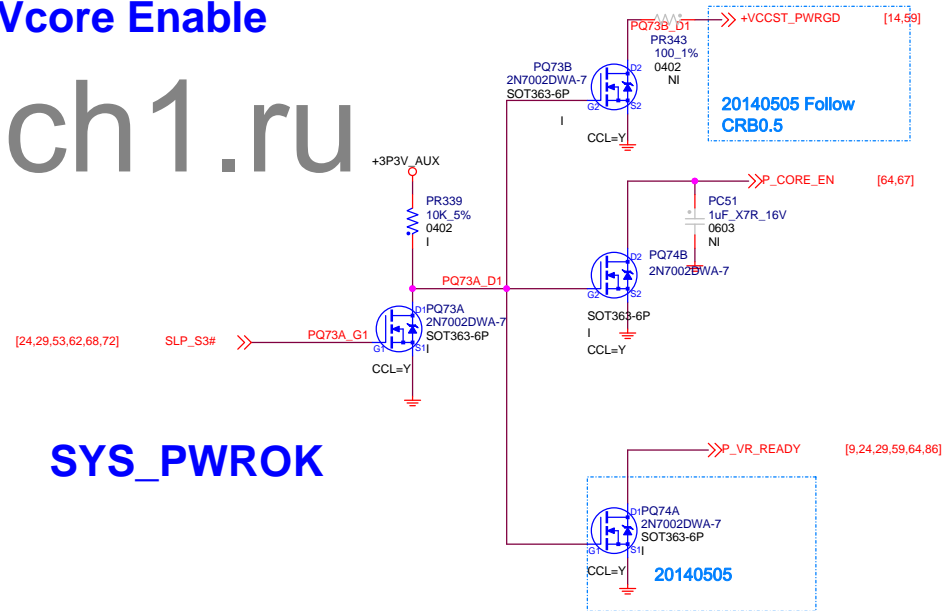
## VCCST\_PWRGD/PCH\_PWROK



## Power Sequence



## Vcore Enable



# SYS\_PWROK



	Title
--	-------

## Power Sequence

DWG NO
--------

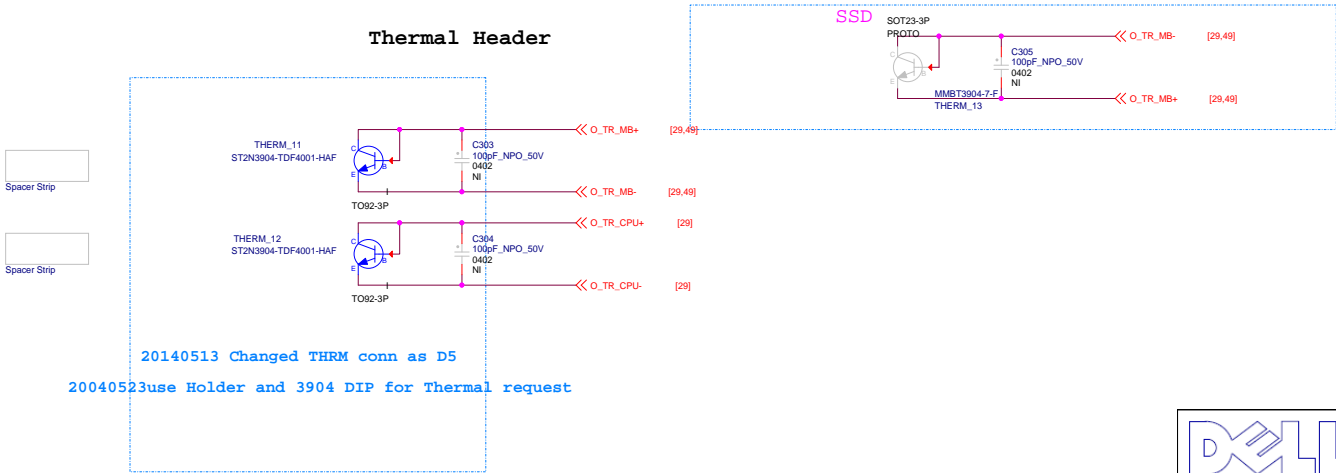
**D7**

Rev	<b>B00</b>
-----	------------

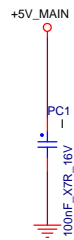
Date: Monday, July 27, 2015

Sheet 48 of 67

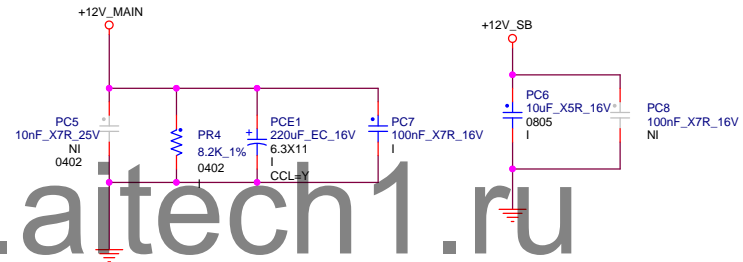
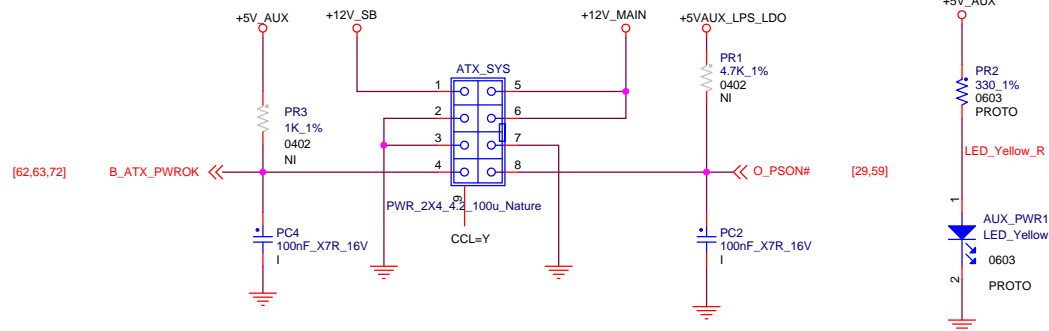
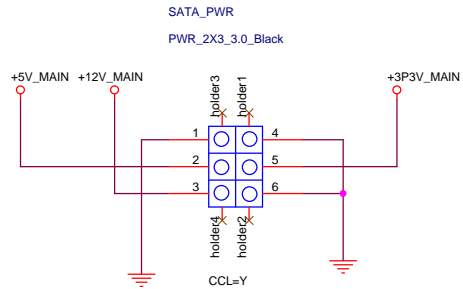
www.aitech1.ru



# ATX POWER CONNECTOR



For ODD and HDD For SFF

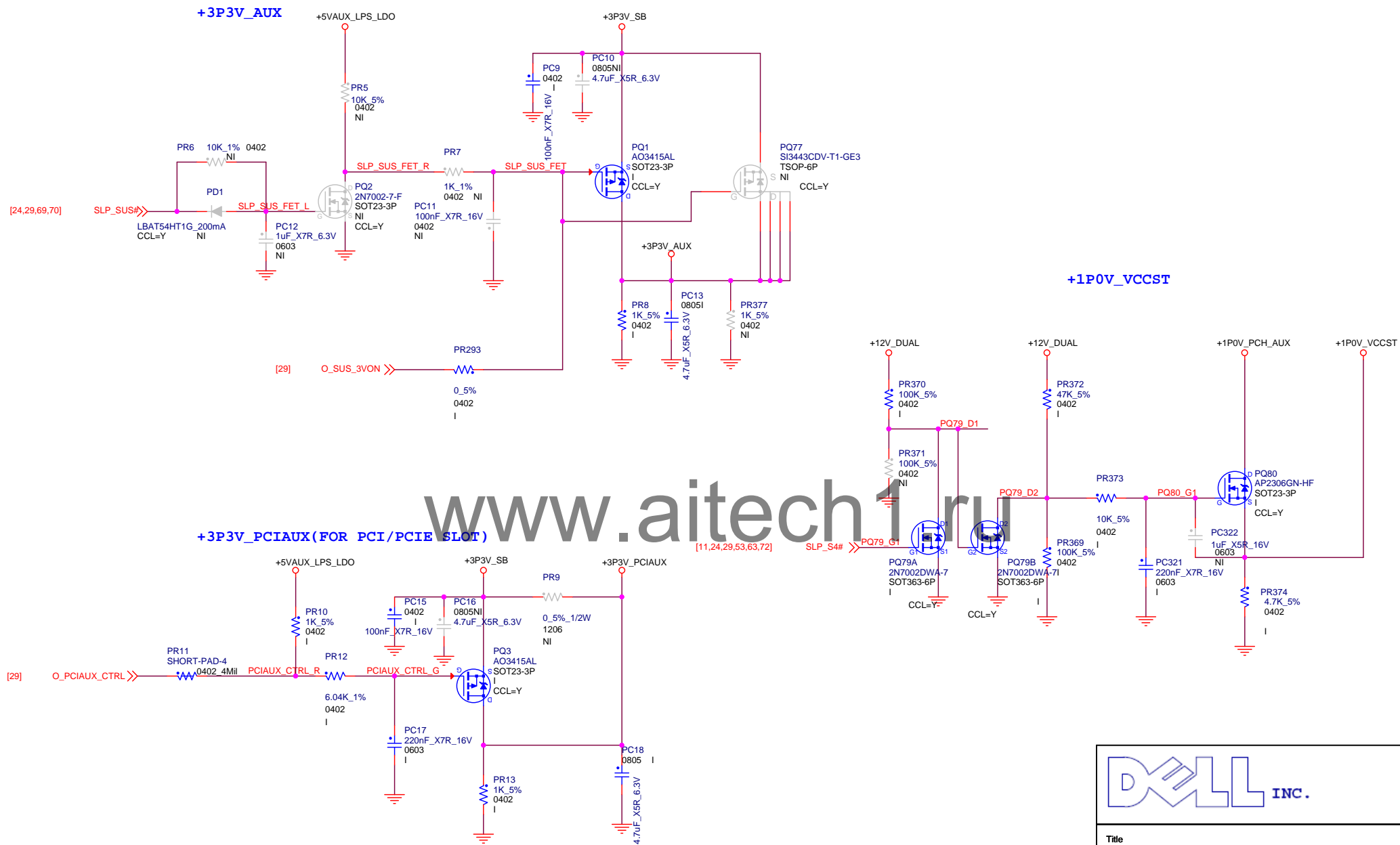


www.aitech1.ru

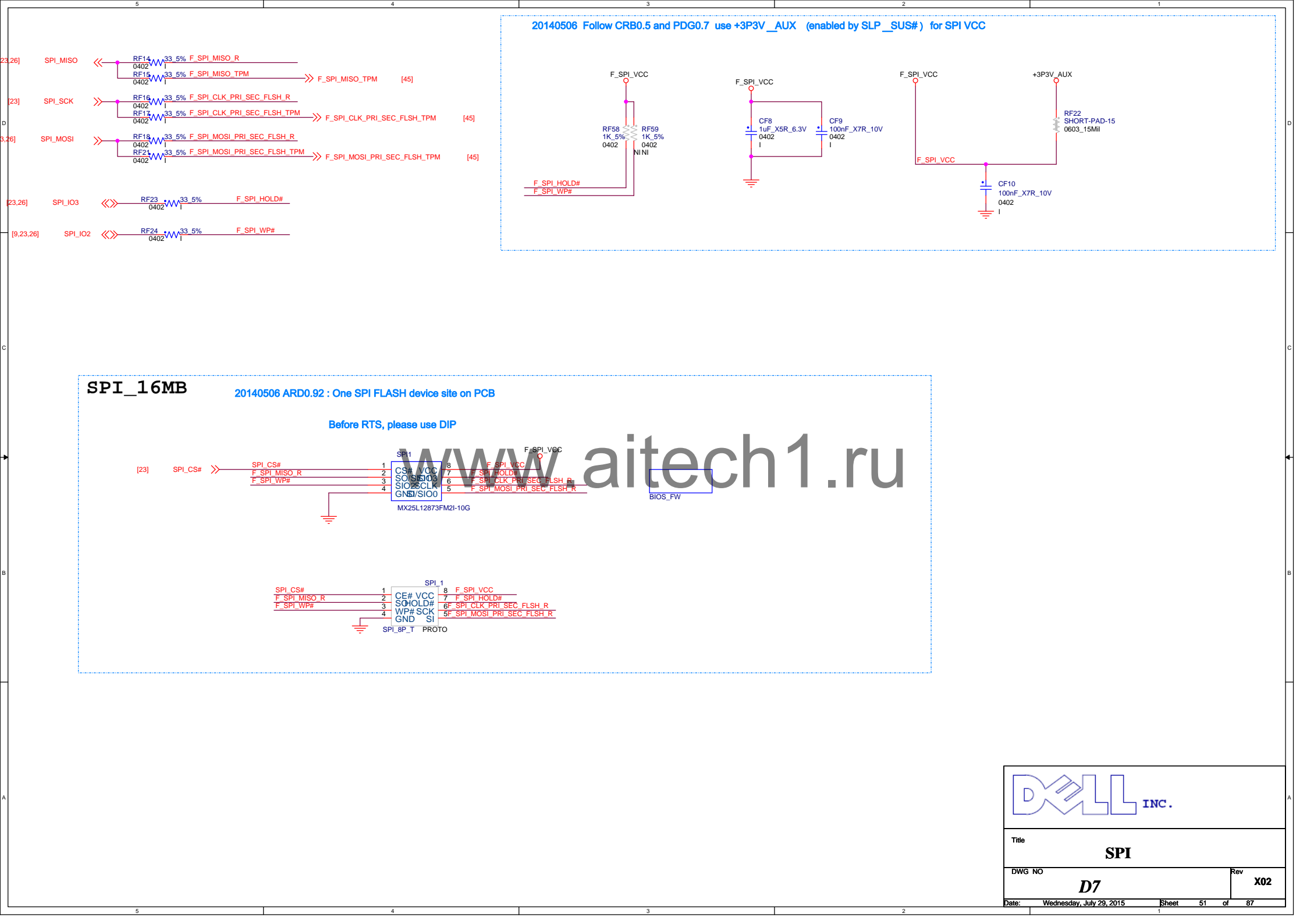


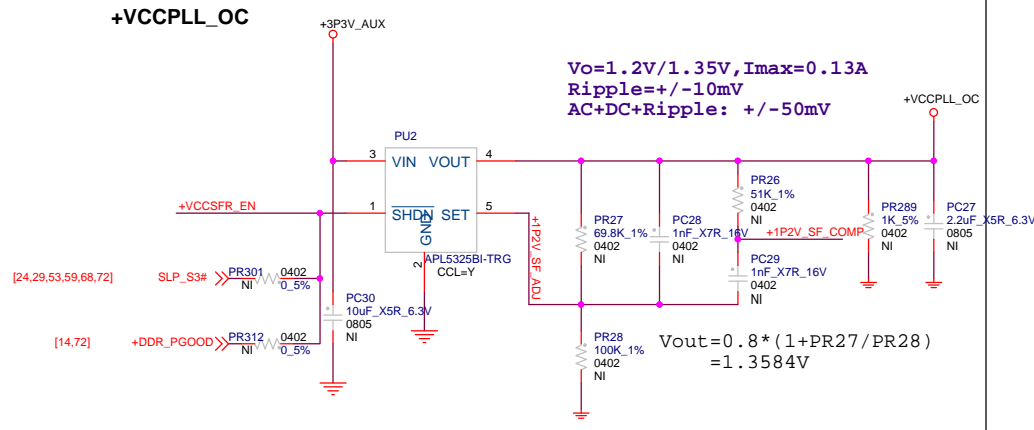
Title		
Power CONN		
DWG NO	Rev	B00
D7		
Date: Monday, July 27, 2015	Sheet	49 of 67



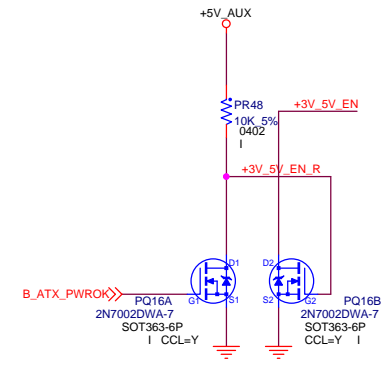
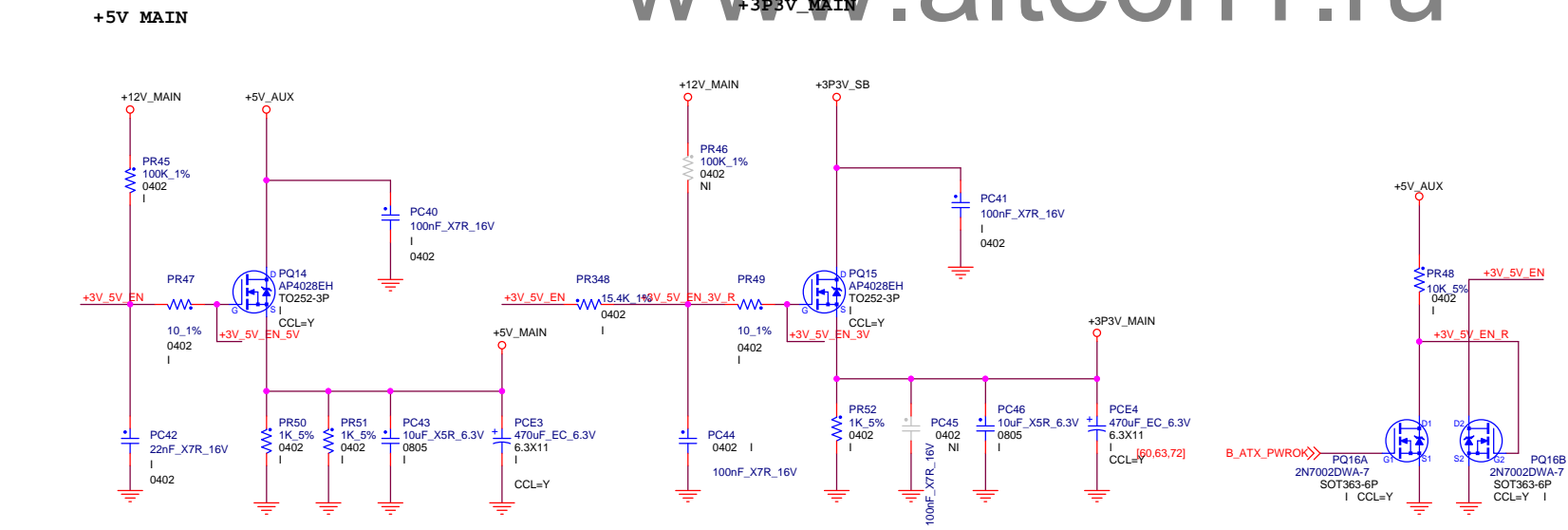


Title		
Power-1: Linear Power-1		
DWG NO		Rev
D7		B00
Date:	Monday, July 27, 2015	Sheet 50 of 67





www.aitech1.ru



Title

**Power-2: Linear Power-2**

DWG NO

**D7**

Date: Monday, July 27, 2015

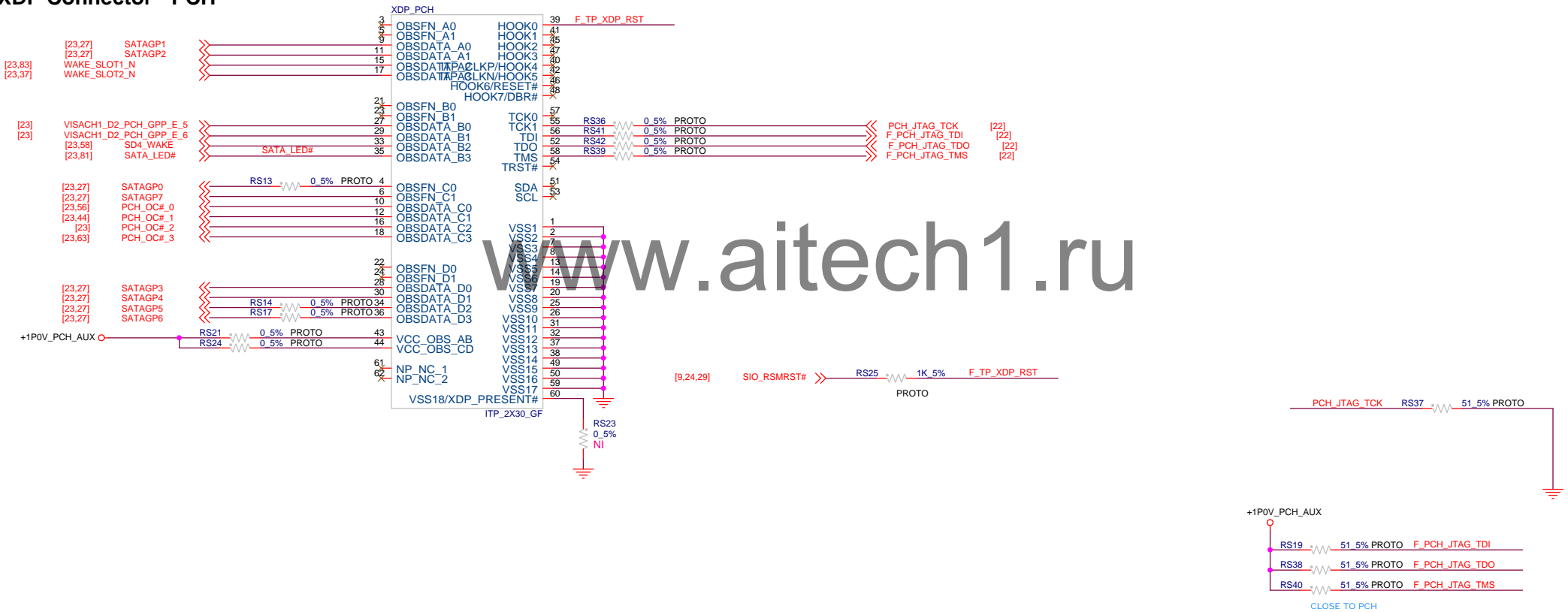
Rev

**B00**

Sheet 51 of 67

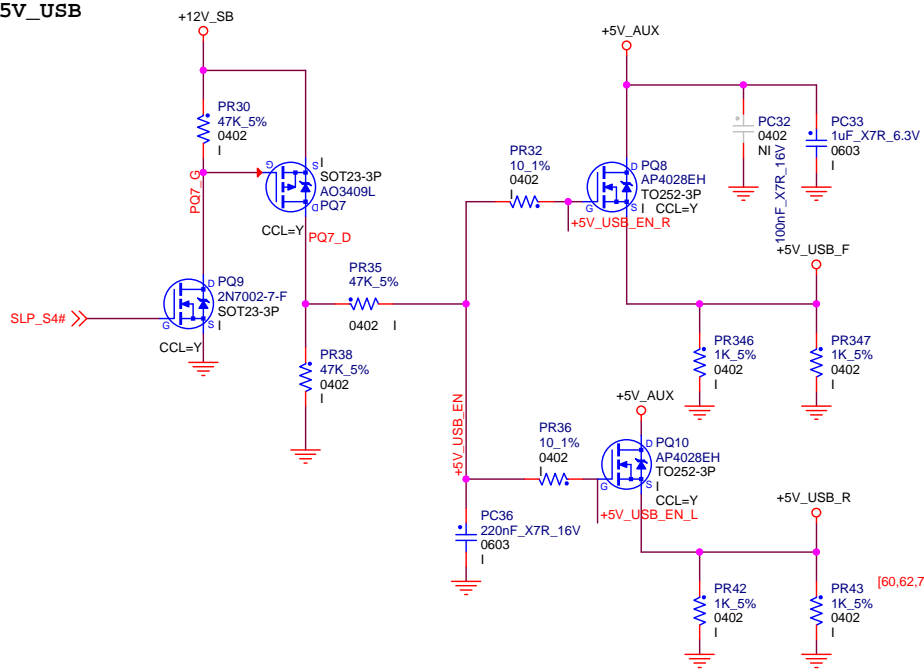
20140505 Remove Duplicated XDP

## XDP Connector - PCH

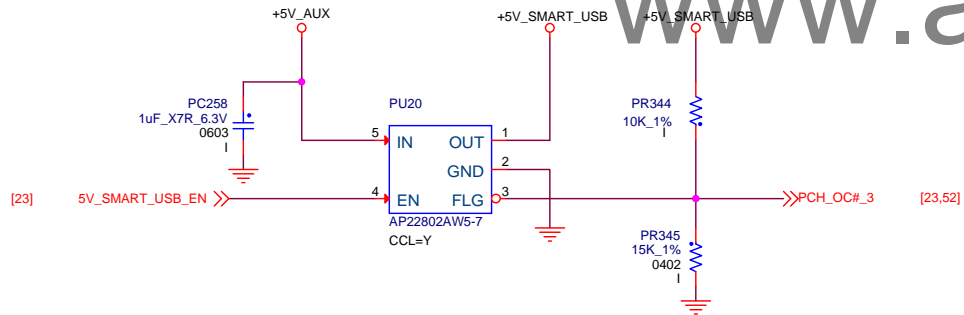


Title			XDP	
DWG NO		D7		Rev
				X02
Date:	Monday, July 27, 2015	Sheet	52	of 87

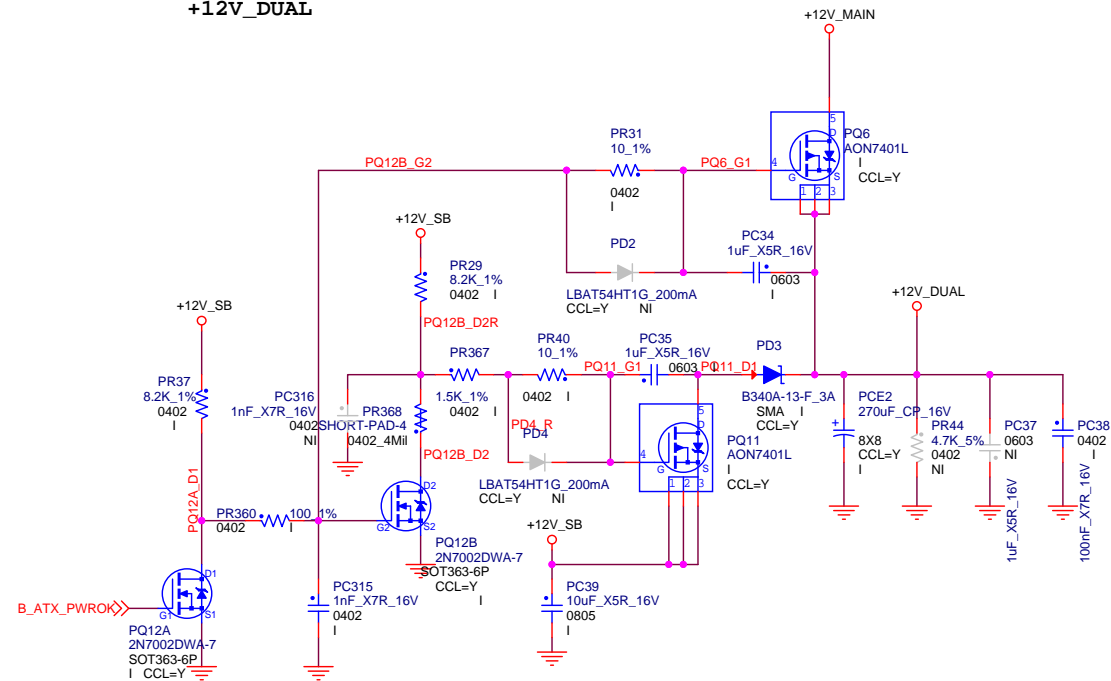
### +5V\_USB



### +5V\_SMART\_USB



### +12V\_DUAL



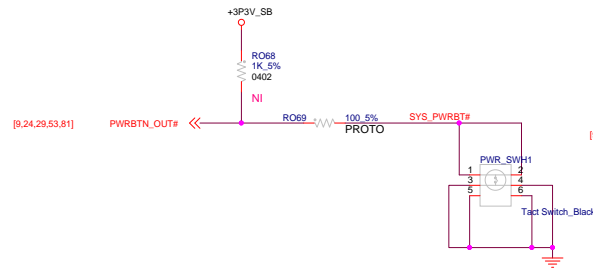
Title  
**Power-3: Linear Power-3**

DWG NO  
**D7**

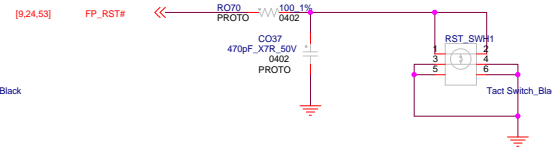
Rev  
**B00**

Date: Monday, July 27, 2015 Sheet 52 of 67

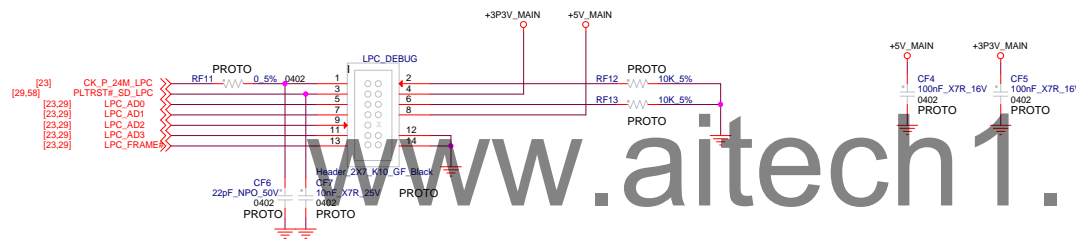
## Power Bottom



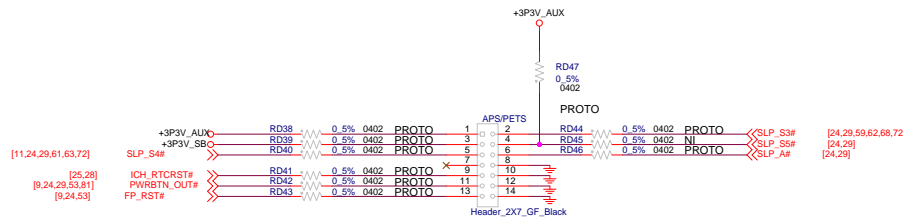
## Reset Bottom



## LPC DEBUG



## APS Debug



Desktop		
APS Connector	Pin	Meaning
Pin 1	VccSus3_3	3.3 V Suspend Power Well
Pin 2	SLP_53#	When asserted (0) system is in S3
Pin 3	VccDSW3_3	Used to determine if system is in Deep Sx
Pin 4	VccSus3_3	When off (0) system is in S5
Pin 5	SLP_54#	When asserted (0) system is in S4
Pin 6	SLP_A#	When asserted (0) ME is in Moff
Pin 7		Unused
Pin 8	GND	Ground
Pin 9	RTCRST#	When asserted (0) CMOS is cleared
Pin 10	GND	Ground for RTCRST#
Pin 11	PWRBTN#	When asserted (0) Power Button Pushed
Pin 12	GND	Ground for PWRBTN#
Pin 13	SYS_RESET#	When asserted (0) Reset Button Pushed
Pin 14	GND	Ground for SYS_RESET#

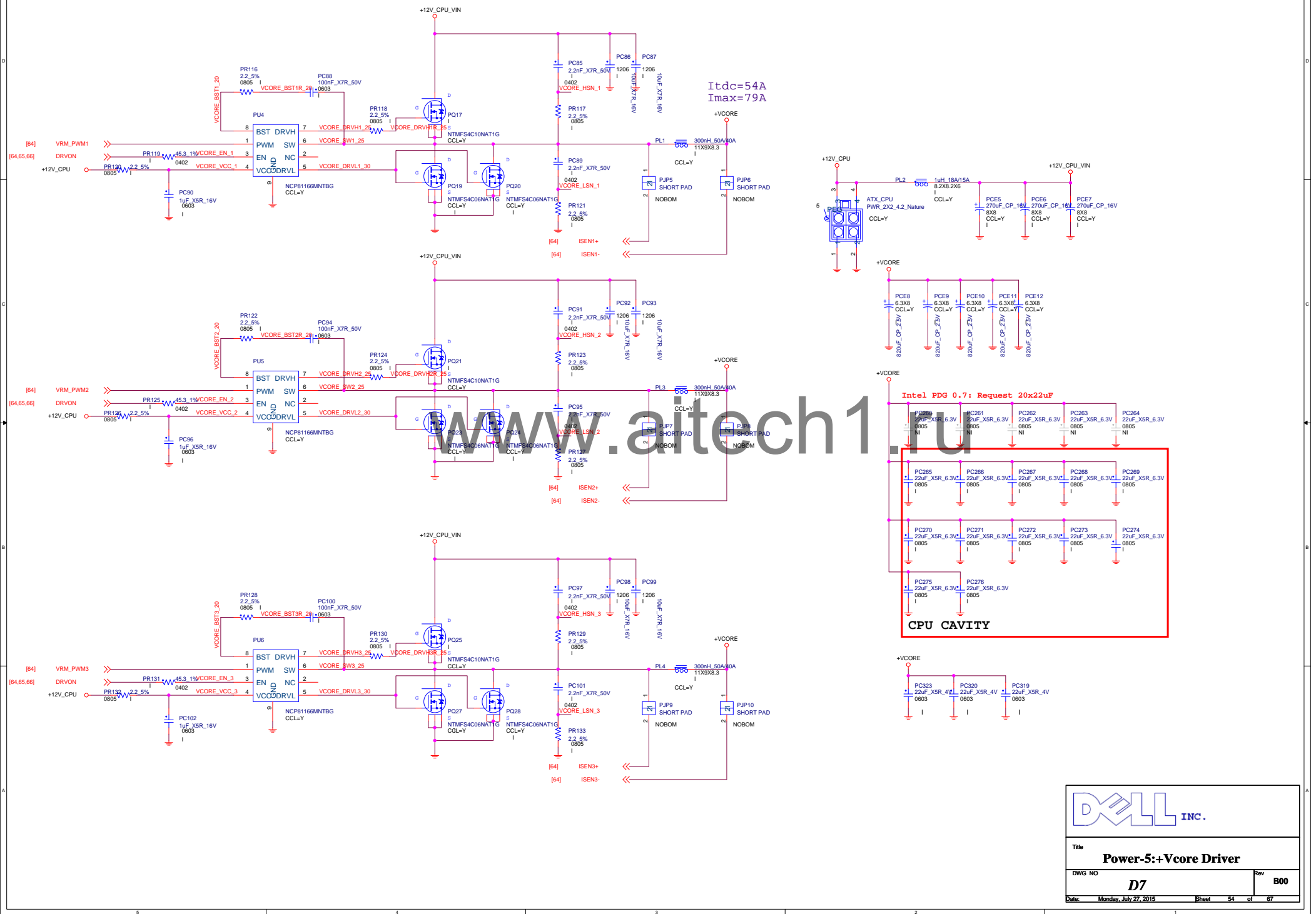




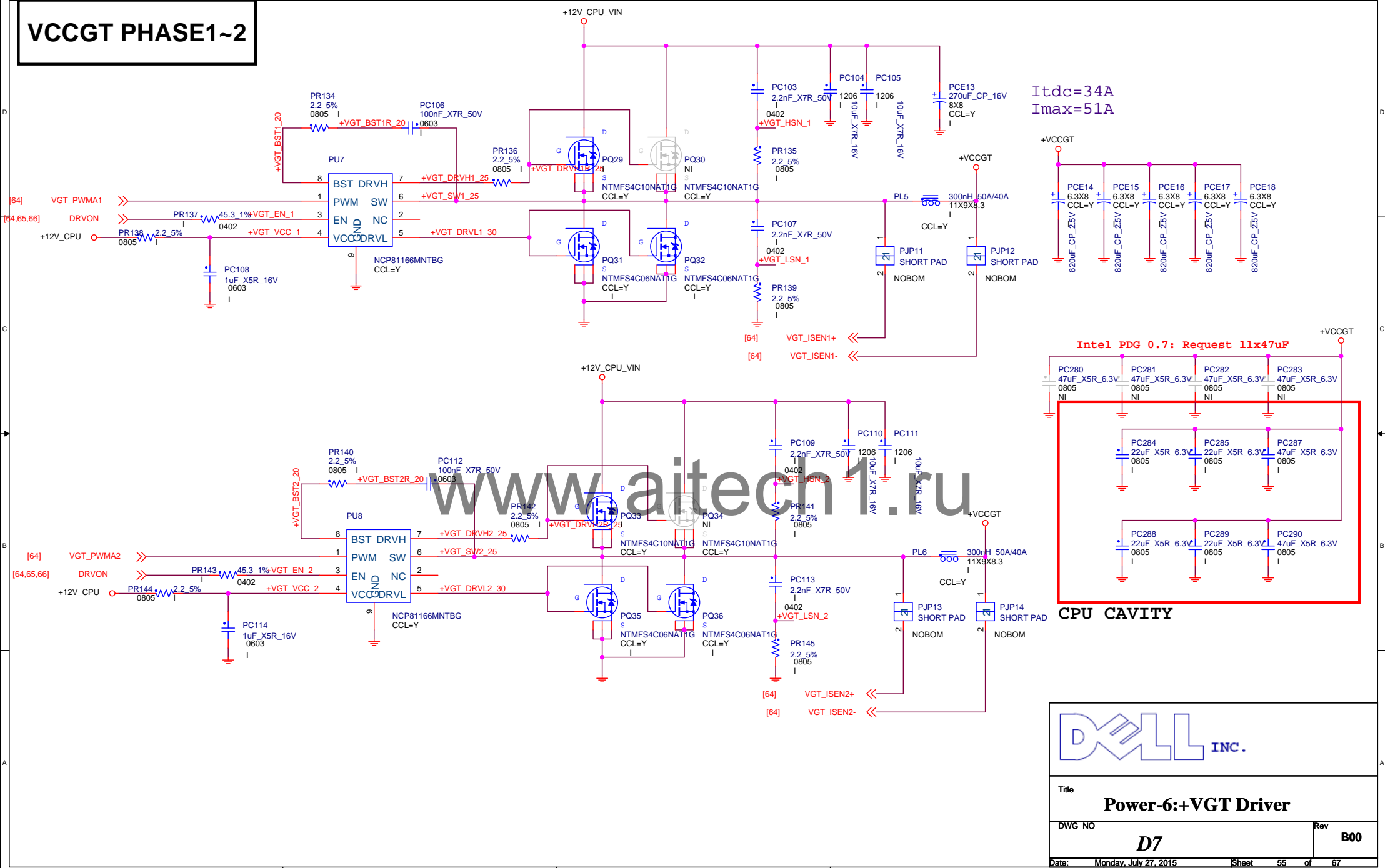




## VCORE PHASE1~3

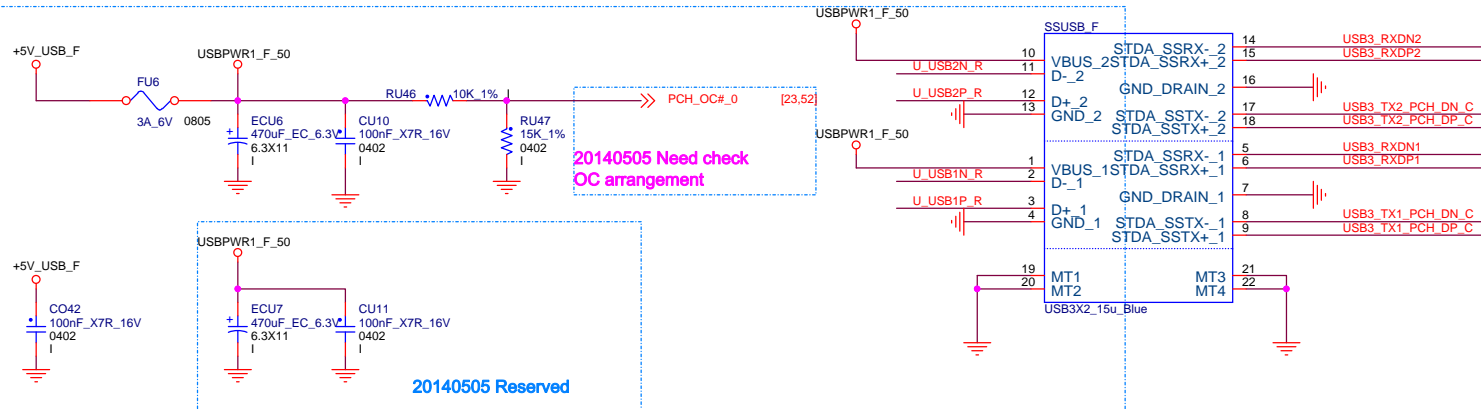


**VCCGT PHASE1~2**

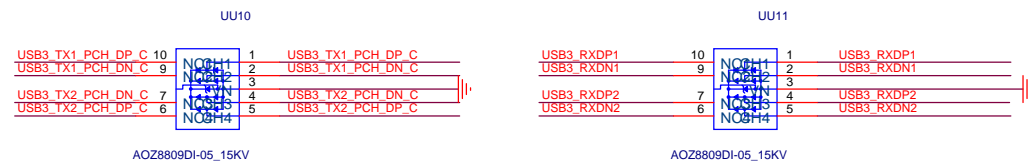
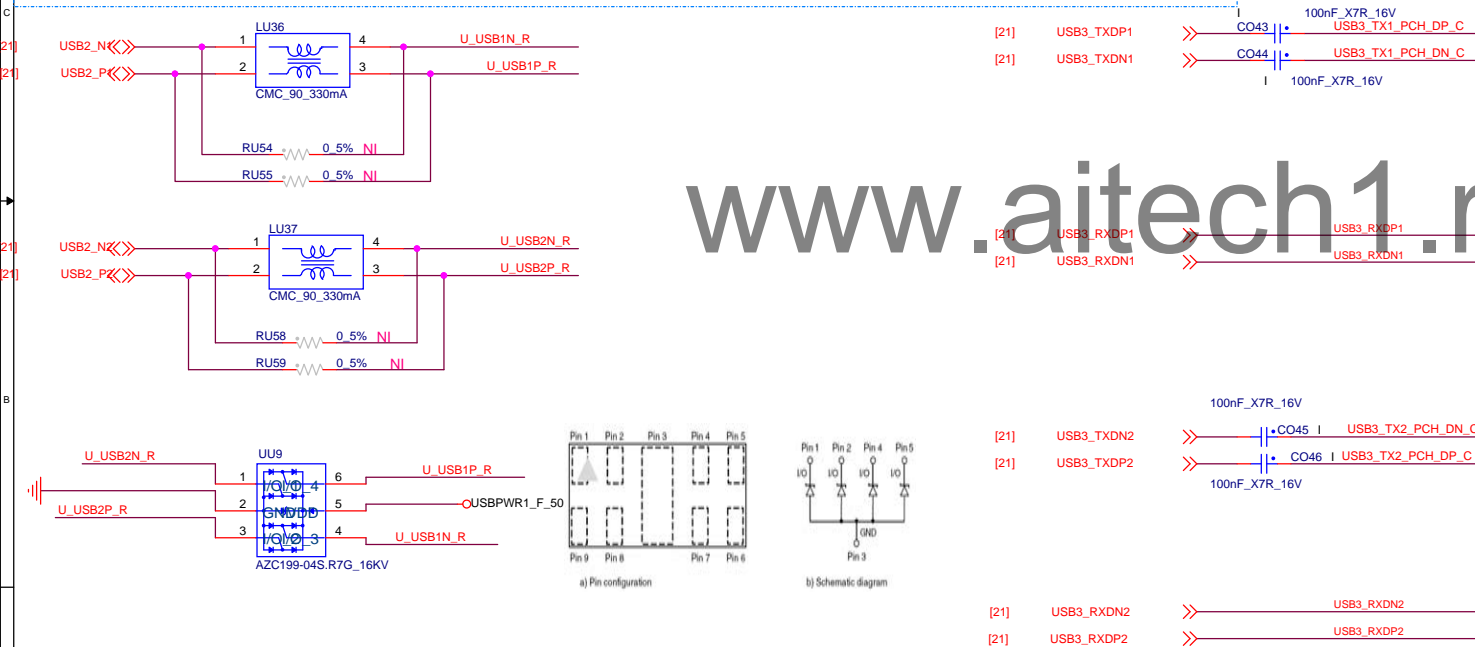


## Front USB/LED Header

**SFF**



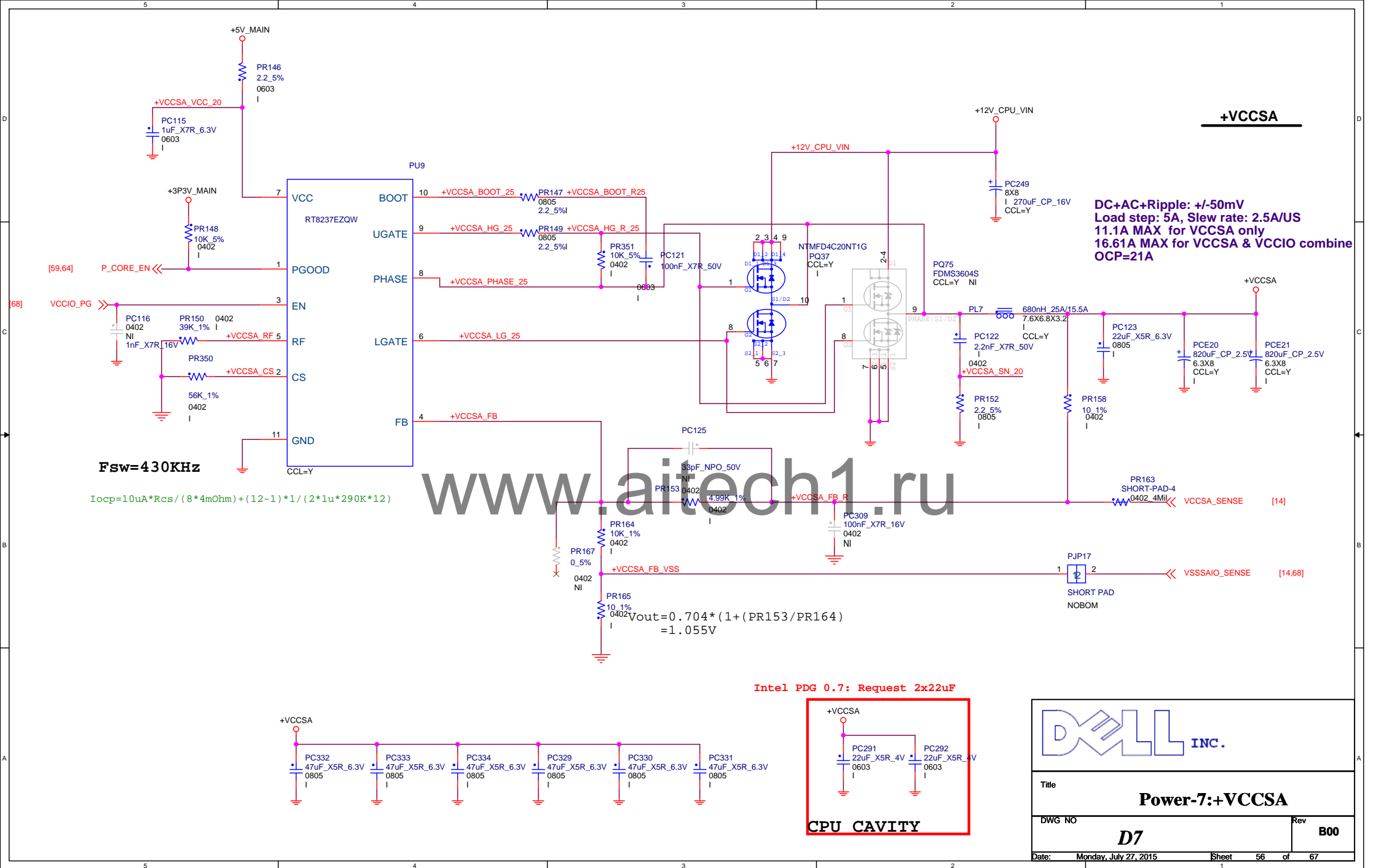
20140505 ARD0.92: Each pair of USB ports will be current limited to 2.5A



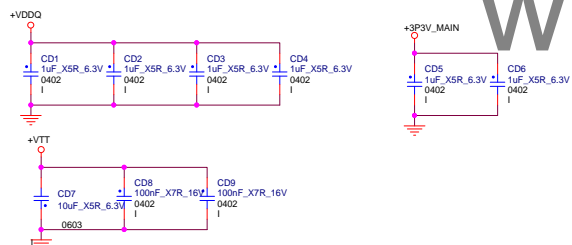
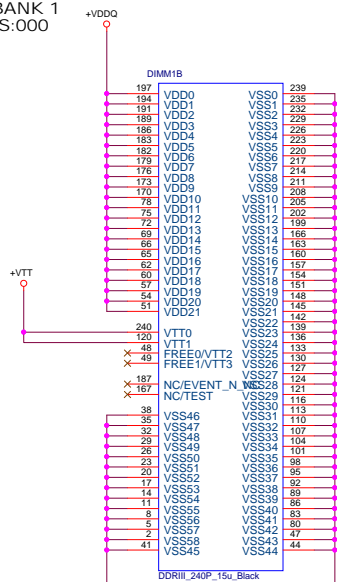
Title	<b>FRONT_USB3.0</b>
-------	---------------------

DWG NO	Rev
<b><i>D7</i></b>	<b>X02</b>

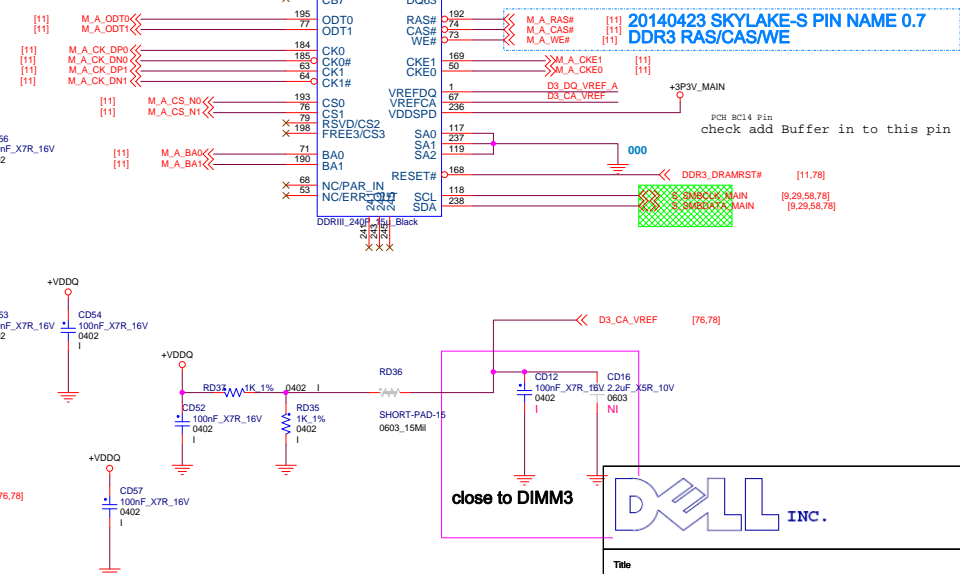
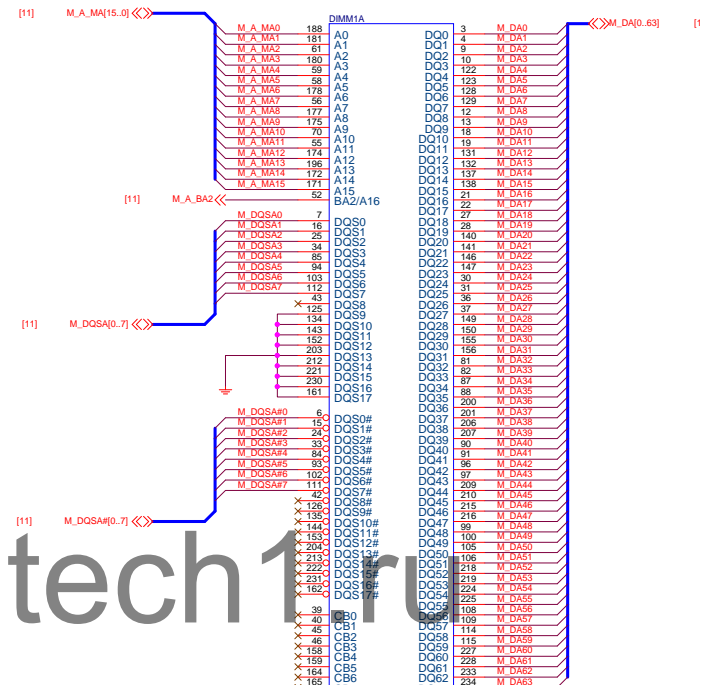
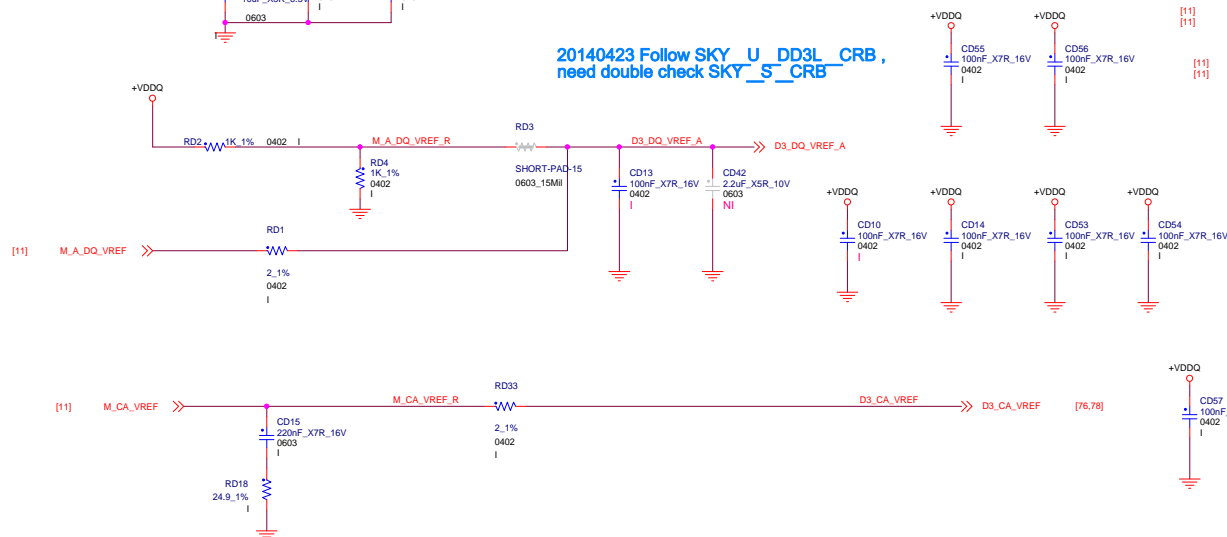
Date: Monday, July 27, 2015 Sheet 56 of 87



CHANNEL A BANK 1  
SMB ADDRESS:000



20140423 Follow SKY U DD3L CRB ,  
need double check SKY S CRB



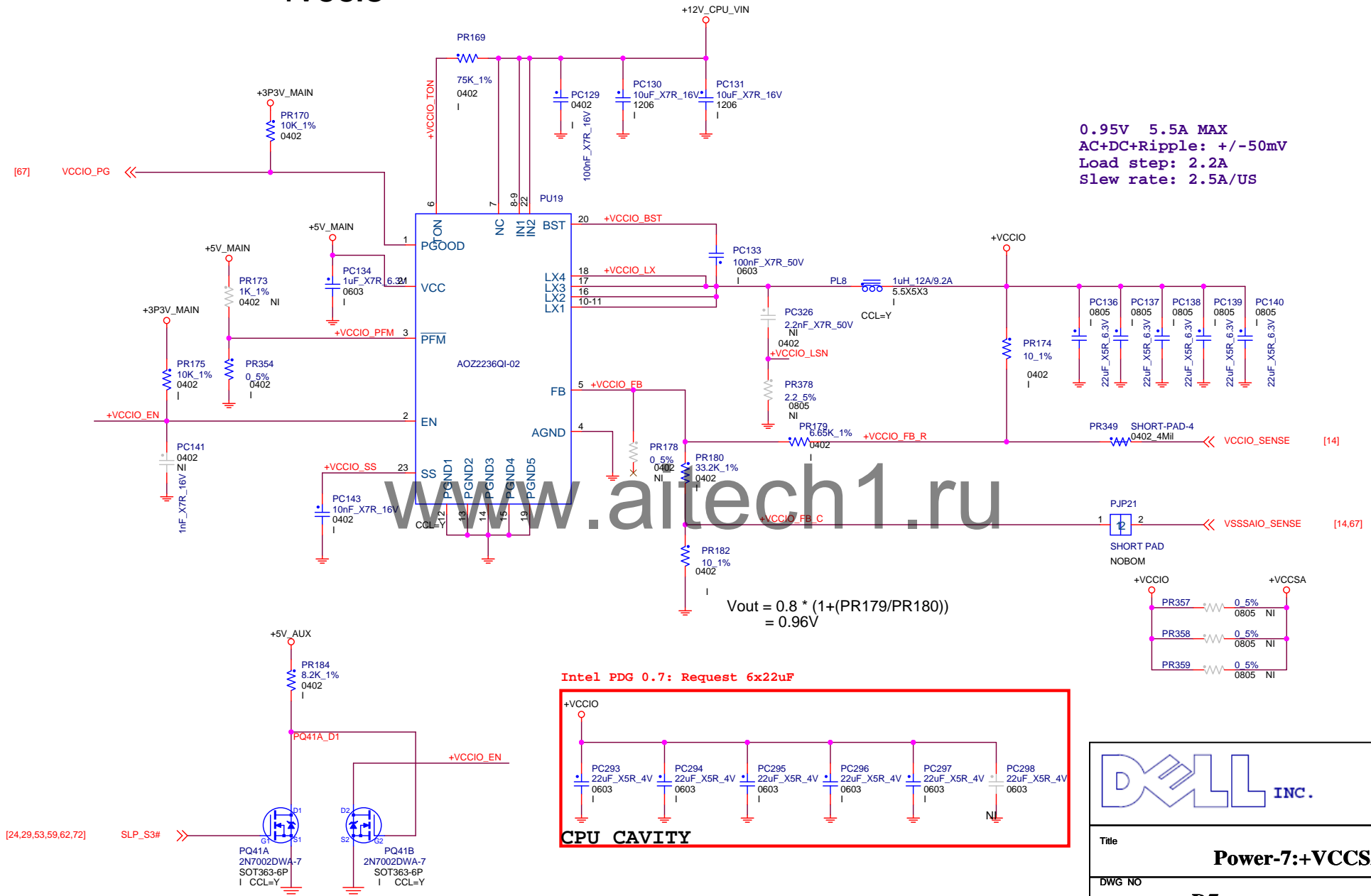
DALL INC.

Title	<b>DDR3 Conn: CHA_1 (DIMM3)</b>
-------	---------------------------------

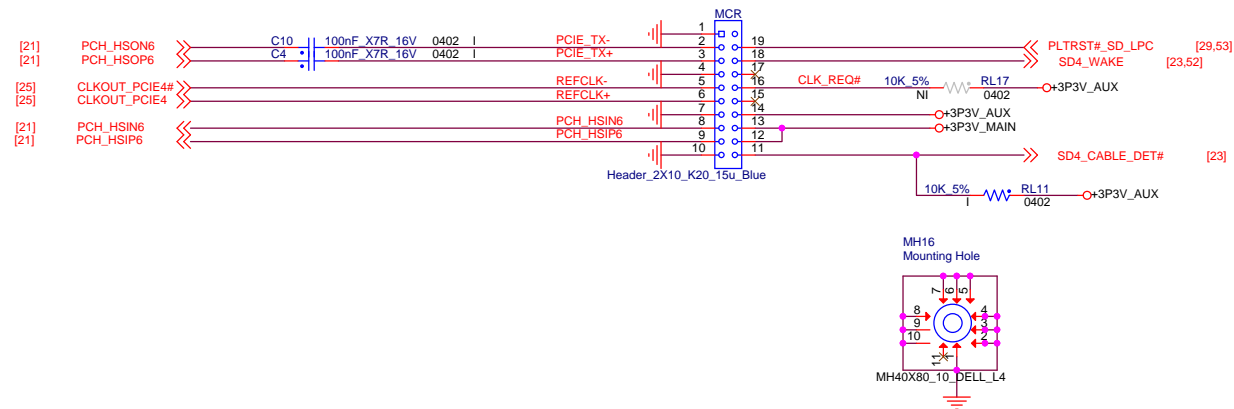
DWG NO	Rev
<b><i>D7</i></b>	<b>X00</b>
Date: Monday, July 27, 2015	Sheet 57 of 65

+VCCIO

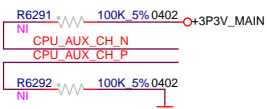
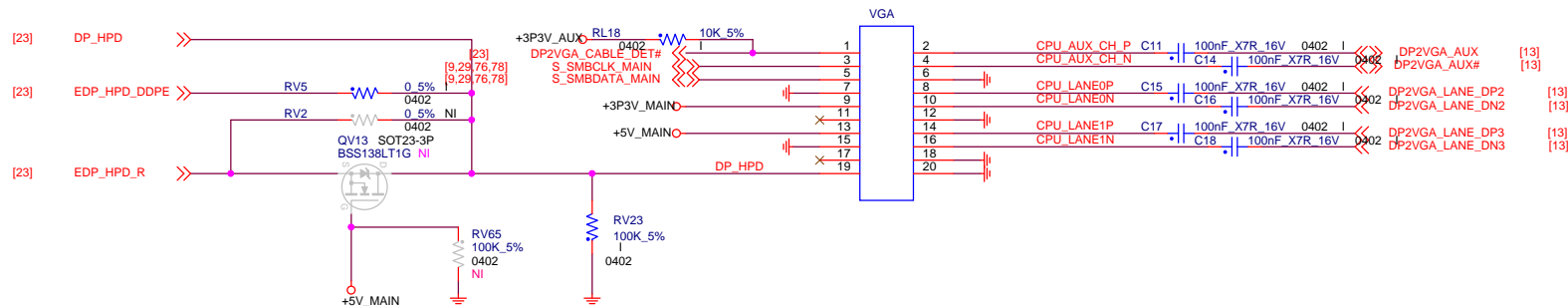
Fsw(KHz)=38000\*Vout/Rton(Kohm)=450KHz



## SD4.0 CONN



eDP to VGA CONN  
M/B part already OK

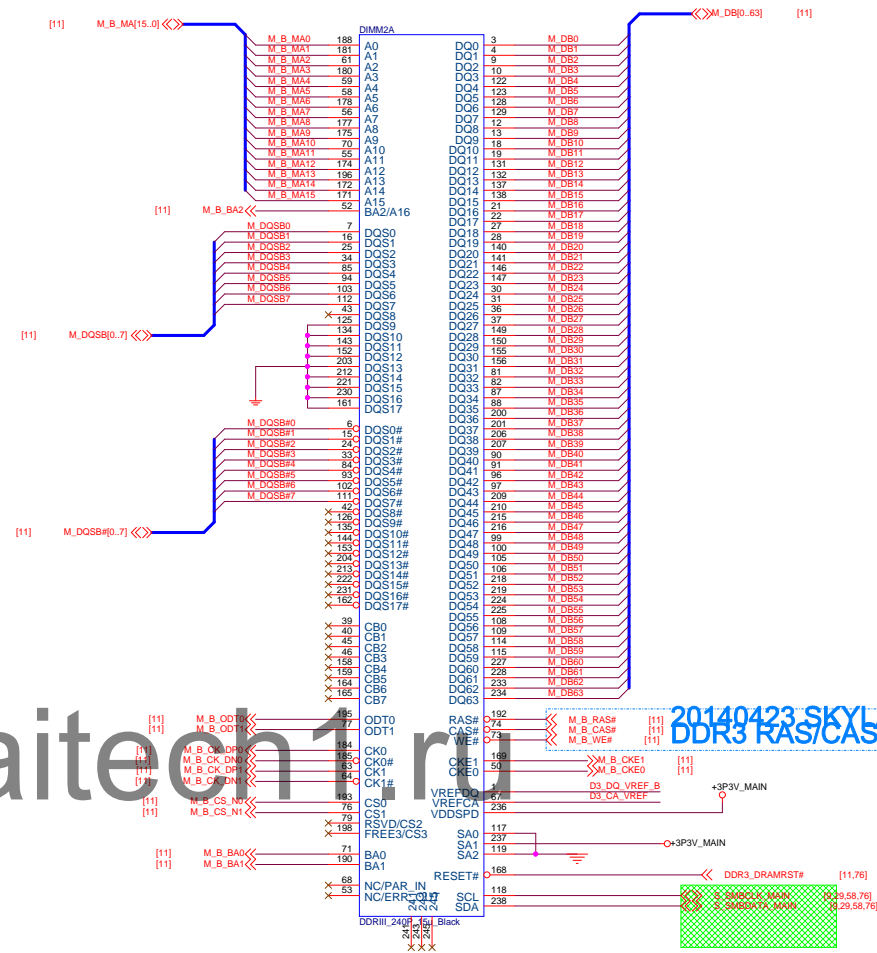
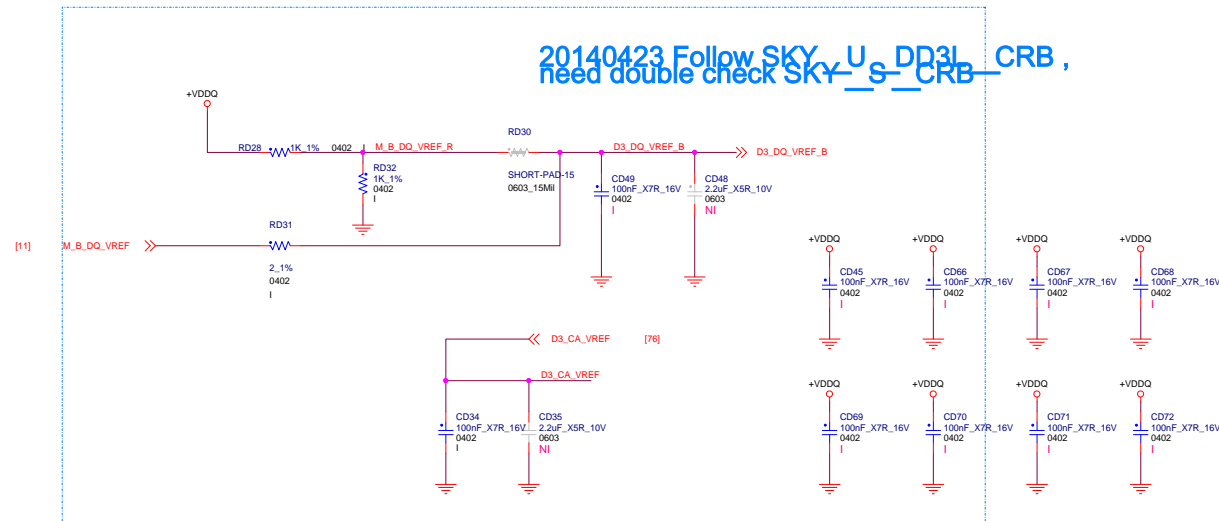
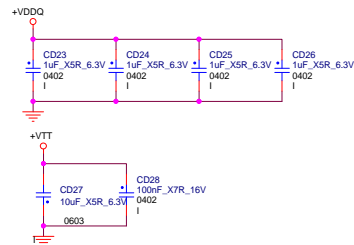
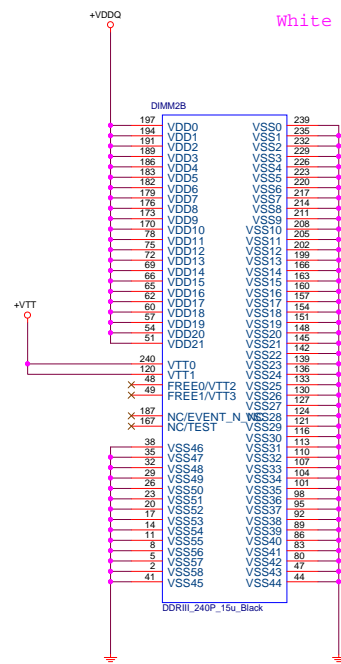


20140515 reserved for AUX



Title		
SD4.0 CON/ DP TO VGA CON		
DWG NO	Rev	
	D7 X02	
Date: Monday, July 27, 2015	Sheet 58	of 87

CHANNEL B BANK 1  
SMB ADDRESS:010



20140423 SKYLAKE-S PIN NAME 0.7

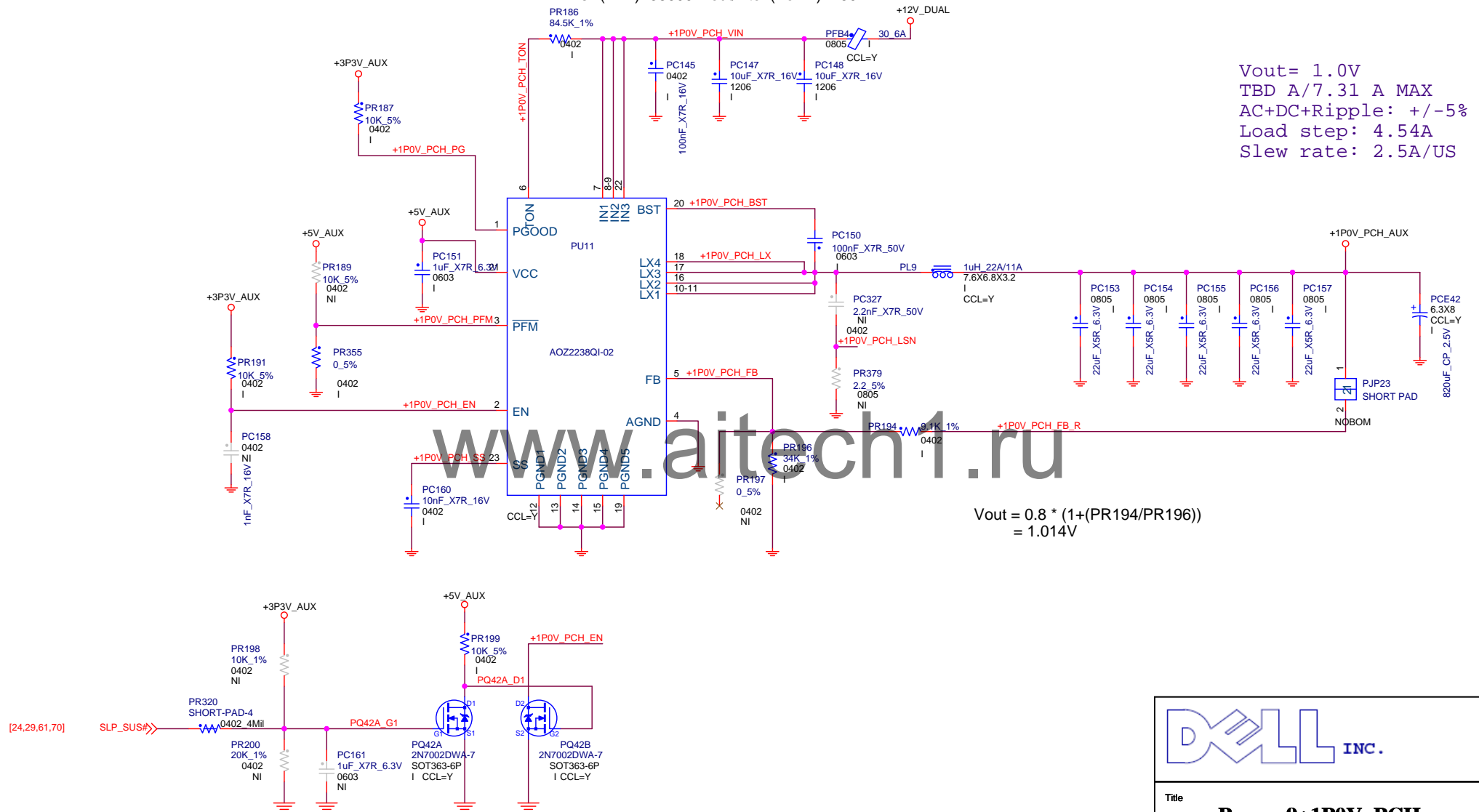
20140423 Follow SKY\_U\_DD3L\_CRB ,  
need double check SKY\_S\_CRB



Title		
<b>DDR3 Conn: CHB_1 (DIMM4)</b>		
DWG NO	<b>D7</b>	Rev <b>X00</b>
Date: Monday, July 27, 2015	Sheet 58	of 65



## +1P0V\_PCH\_AUX

$$F_{sw}(KHz)=38000 \cdot V_{out}/R_{ton}(Kohm)=450KHz$$


DELL INC.

	Title
--	-------

**Power-9+1P0V\_PCH**

DWG NO
--------

***D7***

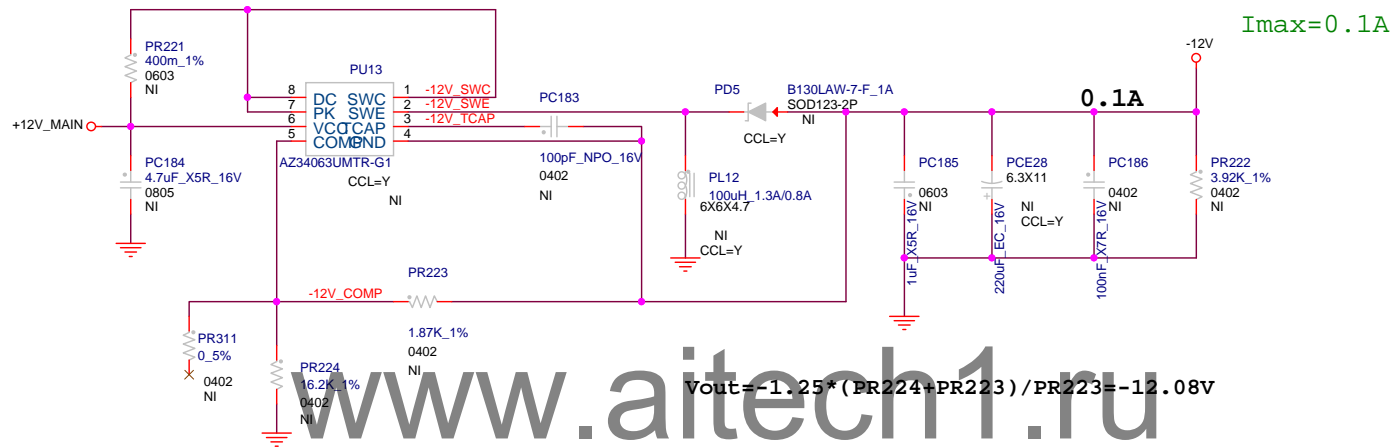
Rev

## B00

Date: Monday, July 27, 2015

Sheet 58 of 67

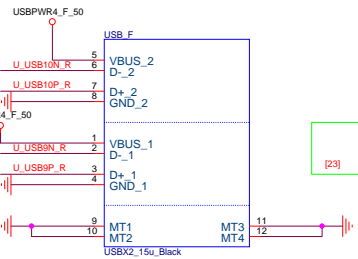




Title			<b>Power-11:-12V</b>		
DWG NO		<b>D7</b>			Rev
					<b>B00</b>
Date:	Monday, July 27, 2015		Sheet	60	of 67

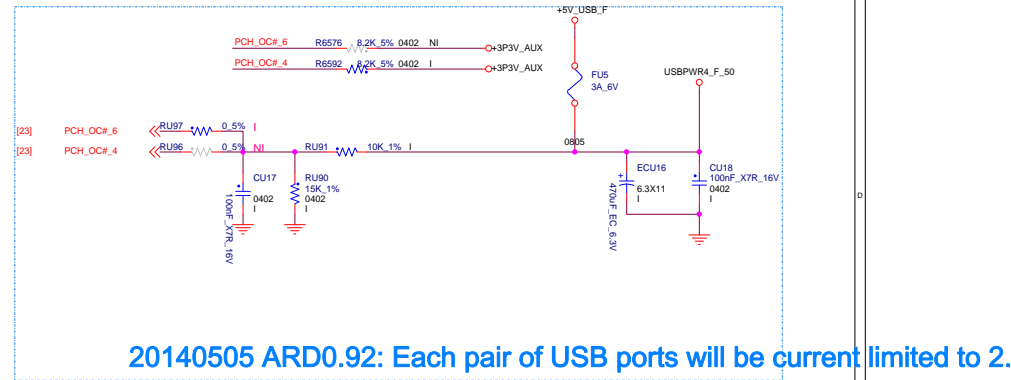
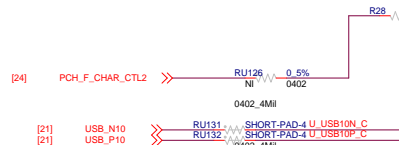


# SFF

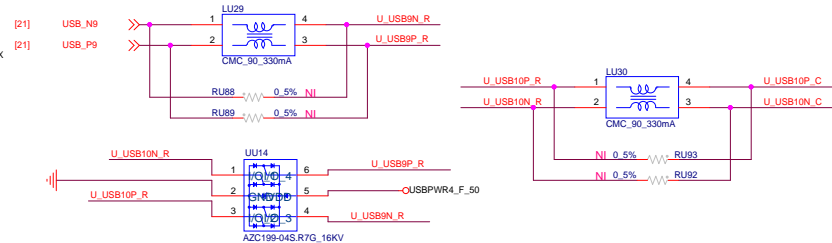


IC on/off  
Hi Lo  
[23] Charge\_power

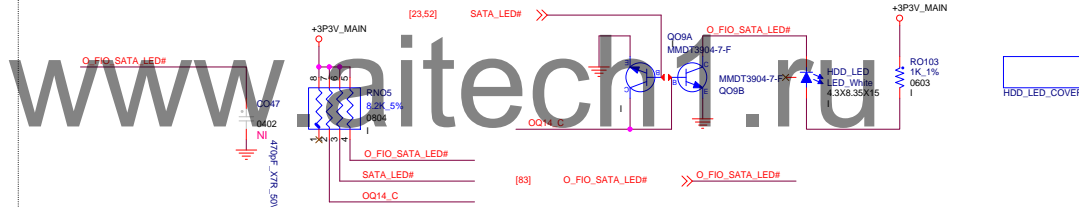
GPIO  
Hi : SDP, CDP  
Lo :DCP, apple  
[23] Charge\_CTL3



20140505 ARD0.92: Each pair of USB ports will be current limited to 2.5A



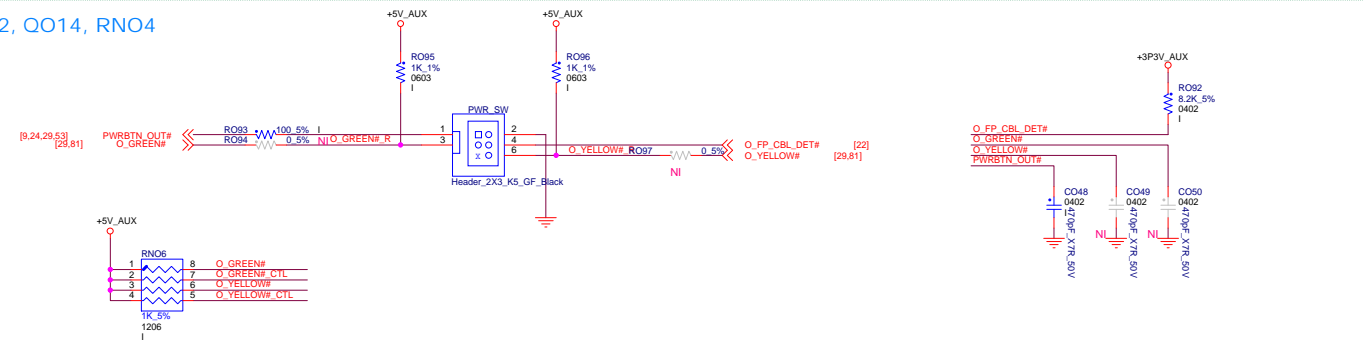
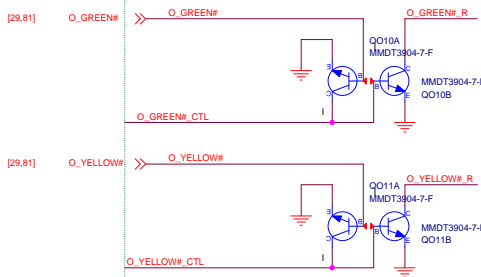
## SATA LED



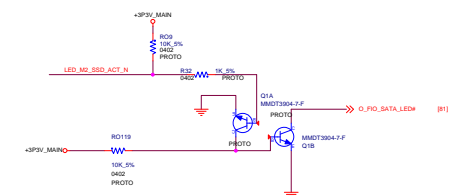
## POWER SWITCH Header

20120521: Add QO12, QO14, RN04, RO84, RO86 for Power LED control

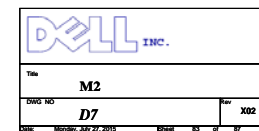
If stuffed RO84, RO86 ; Dummy QO12, QO14, RN04

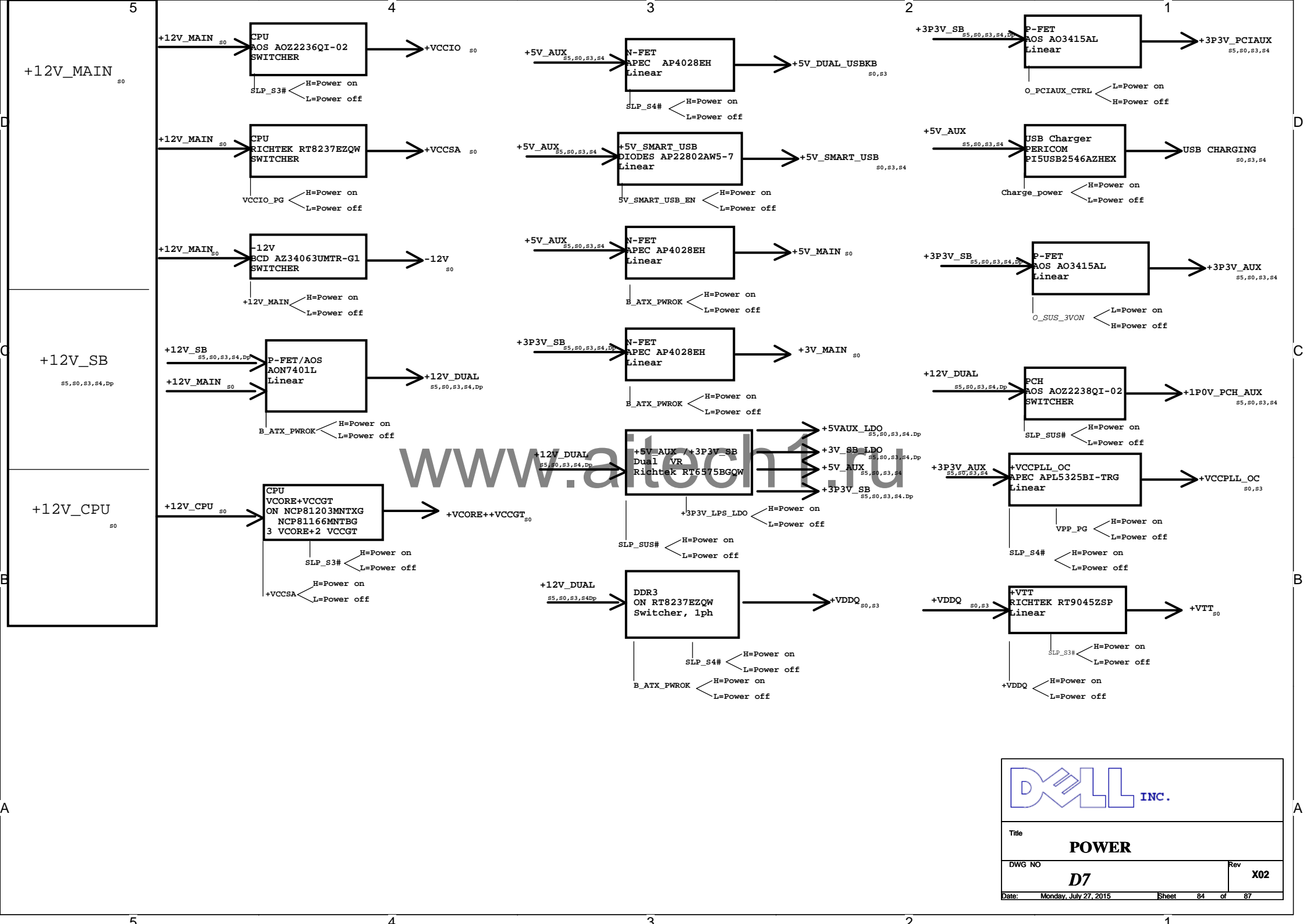






[www.aitech1.ru](http://www.aitech1.ru)



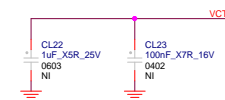
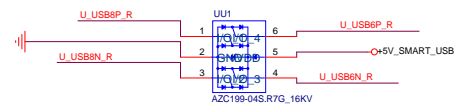
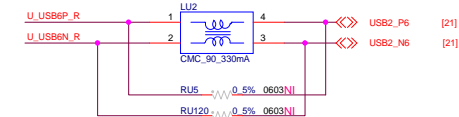
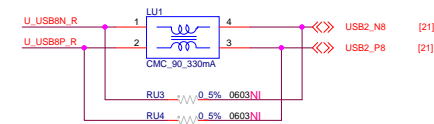
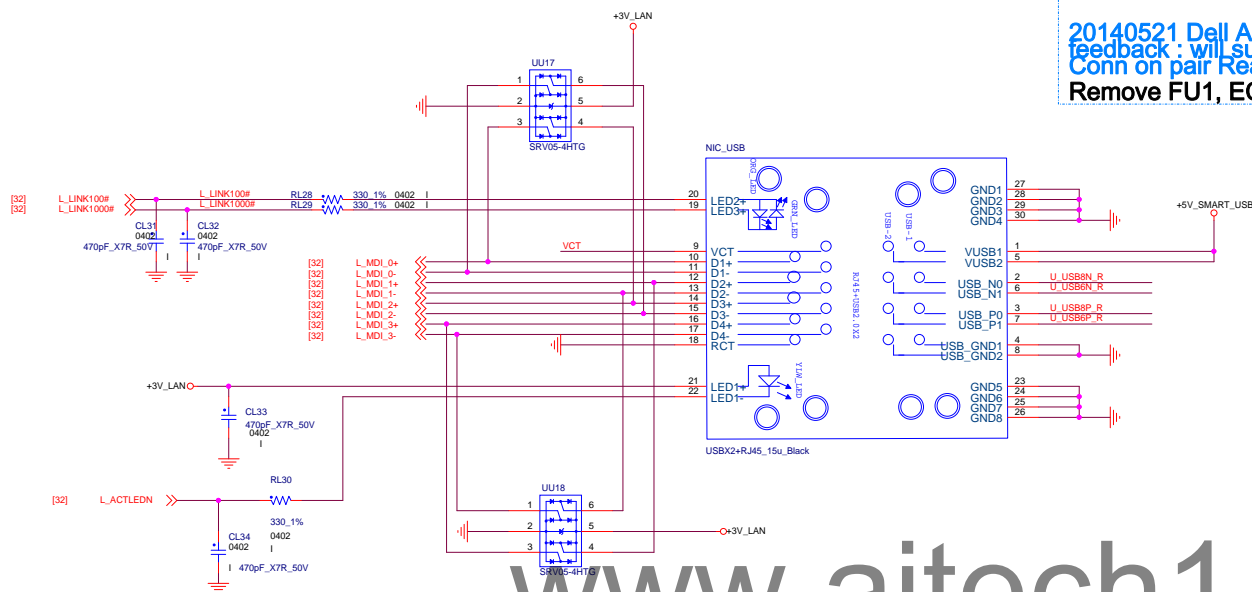




# LAN CONNECTOR

20140509 ARD1.01: Support Smart Power On Conn  
20140514 FU1 need change to 1.1A

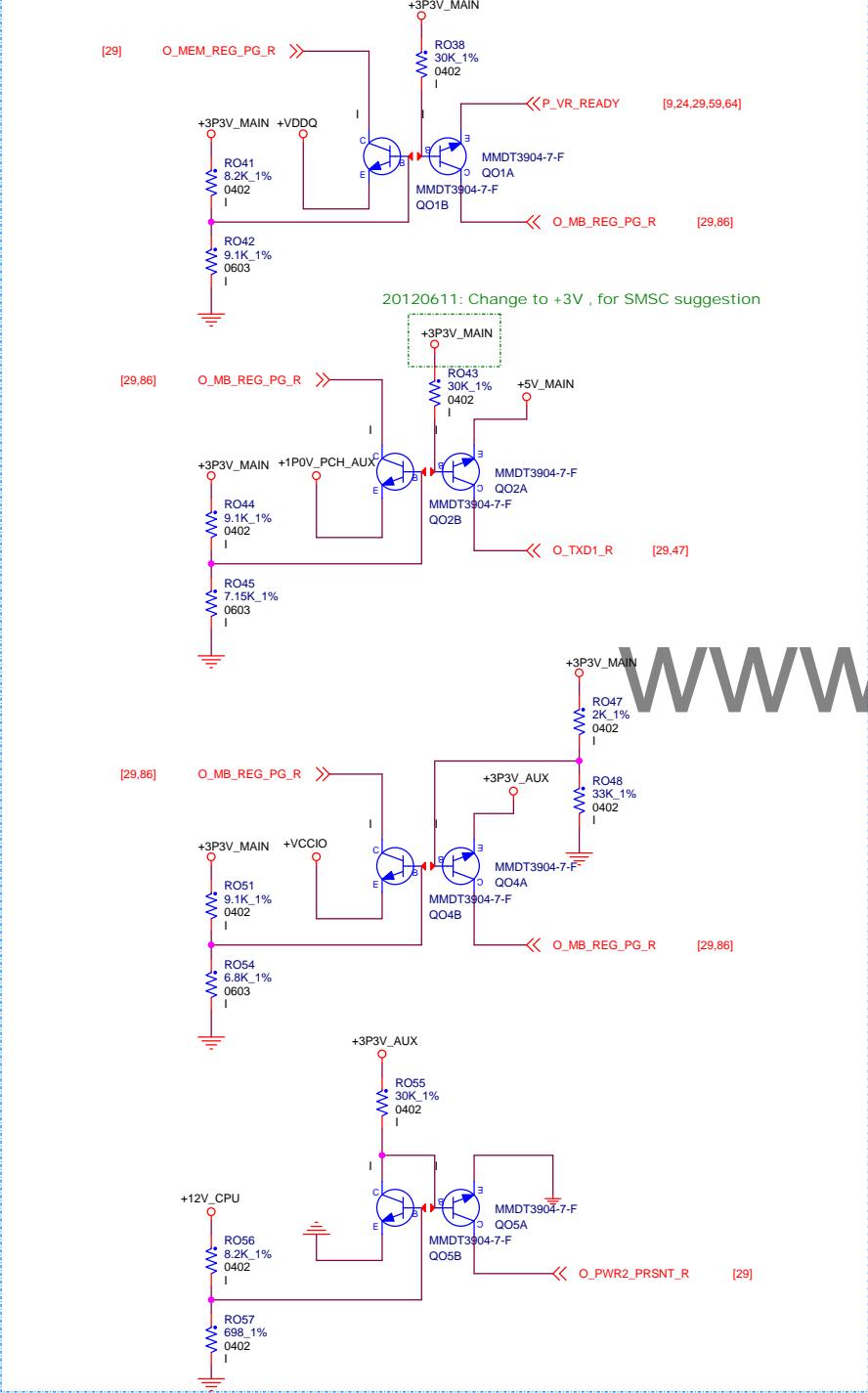
20140521 Dell ARD1.01 Q&A  
feedback : will support Smart USB  
Conn on pair Rear USB2.0 port.  
**Remove FU1, ECU1, CU1, RU1, RU2**



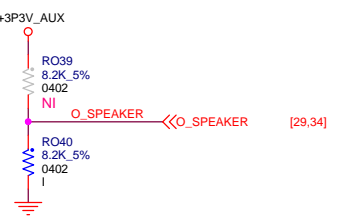
www.aitech1.ru

5555 PRE-POST DIAG Monitor

20140429 Chaned monitor power for SKYLAKE , MUST double confirm with SMSC



SIO STRAPING



SIO STRAPING

	SPEAKER	
	Diag_En	
PULL HIGH	Disable	
PULL LOW	Enable	

SIO5555 V5\_ALW Monitor

